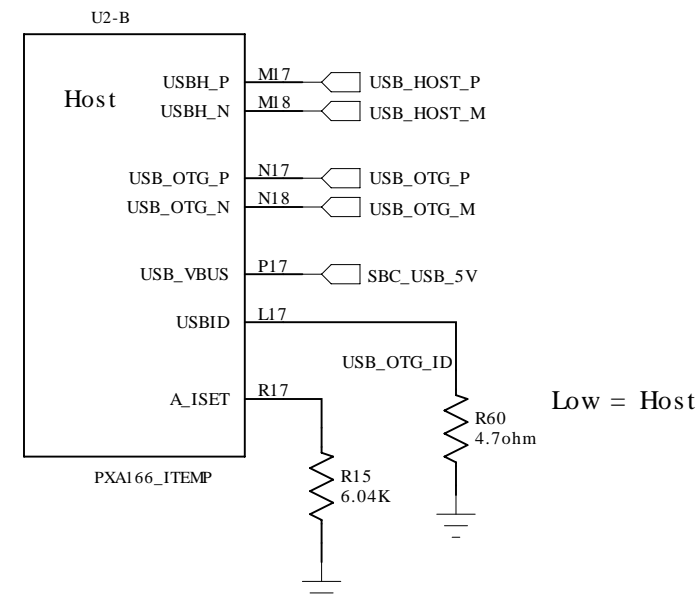
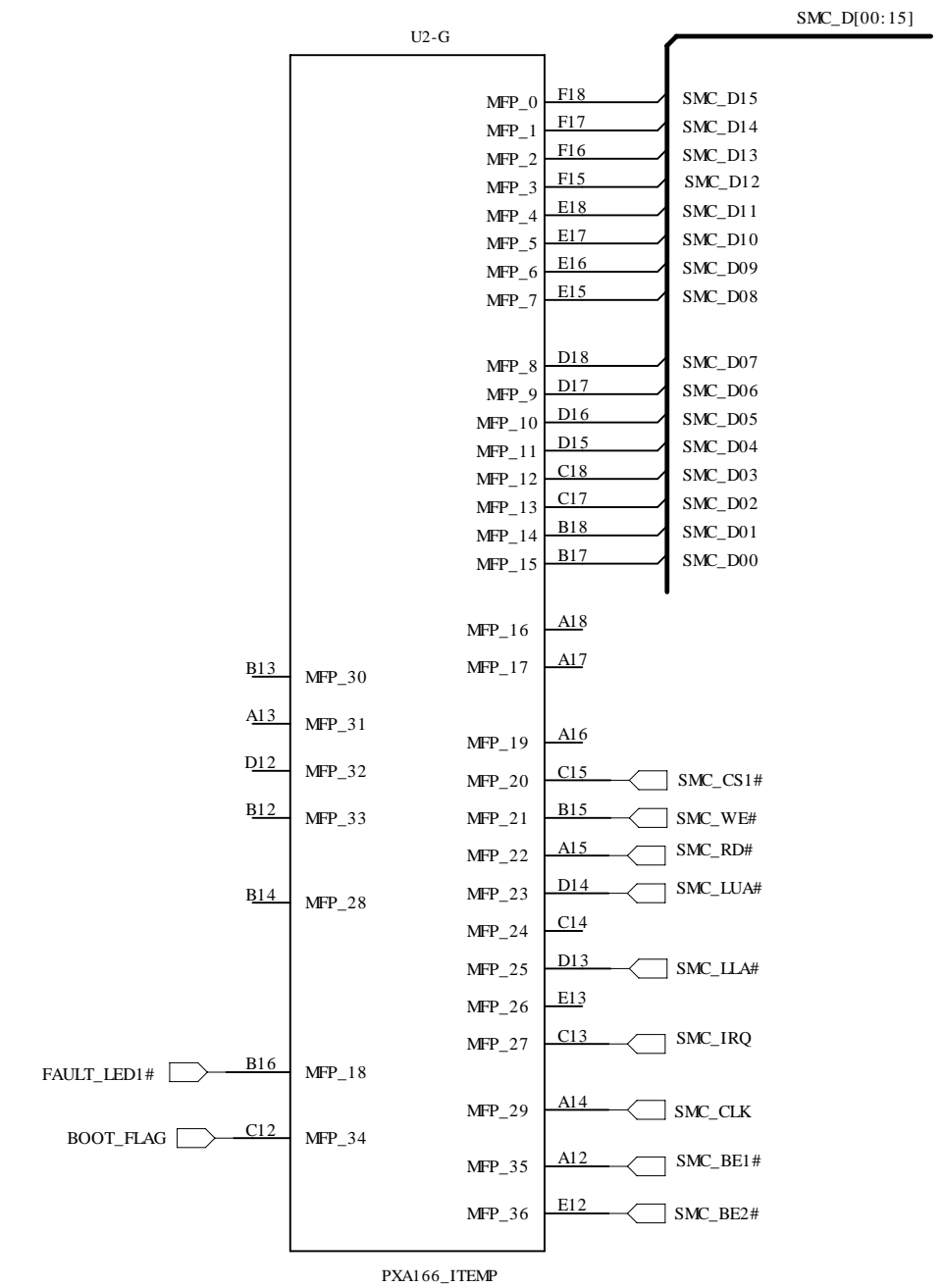


PXA166 800 MHz - PXA168 1066 MHz

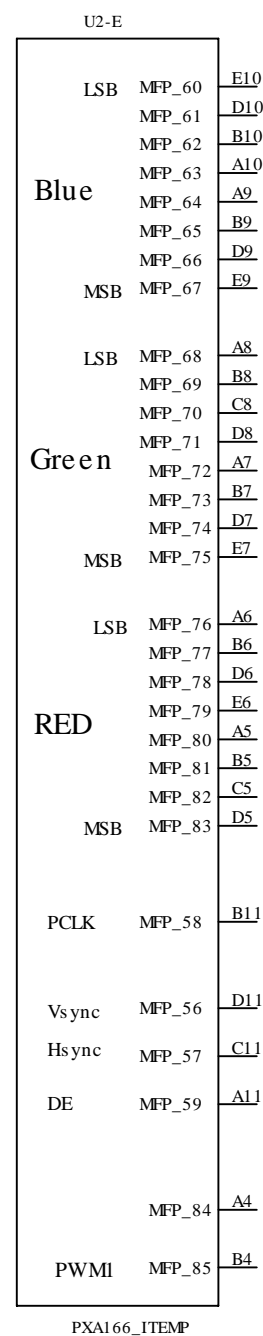
USB Ports



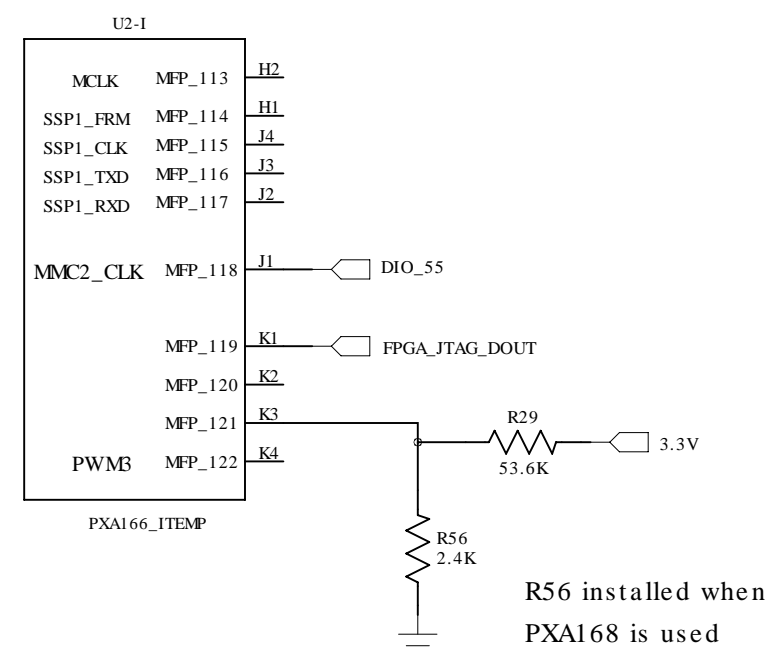
SMC Bus



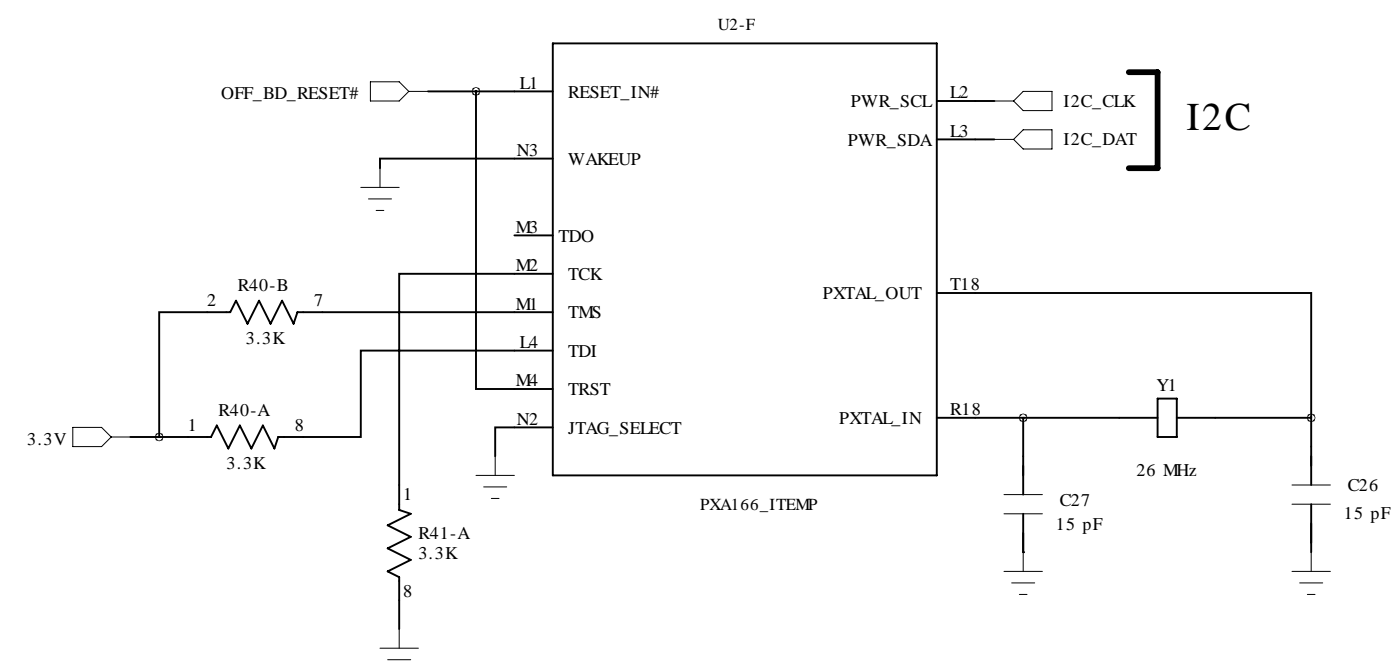
LCD



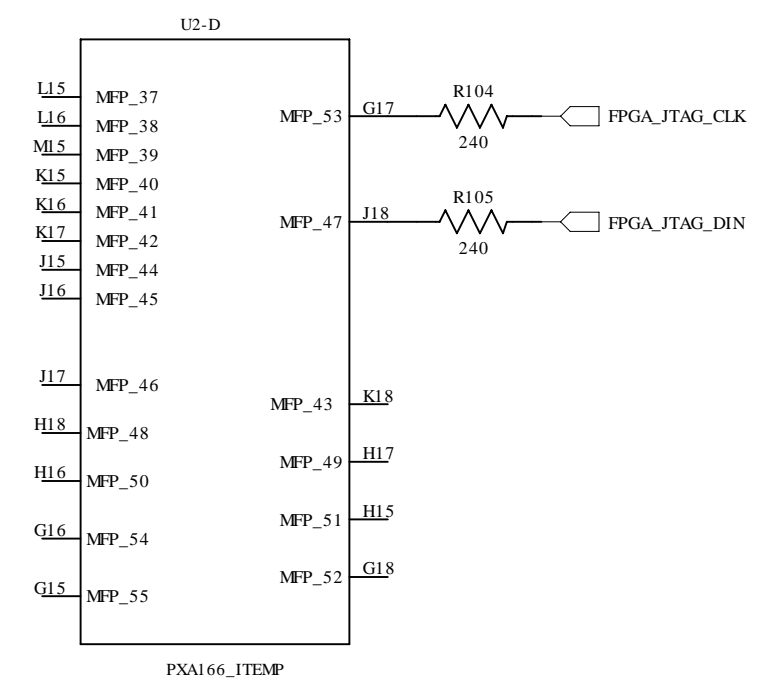
I2S



Control



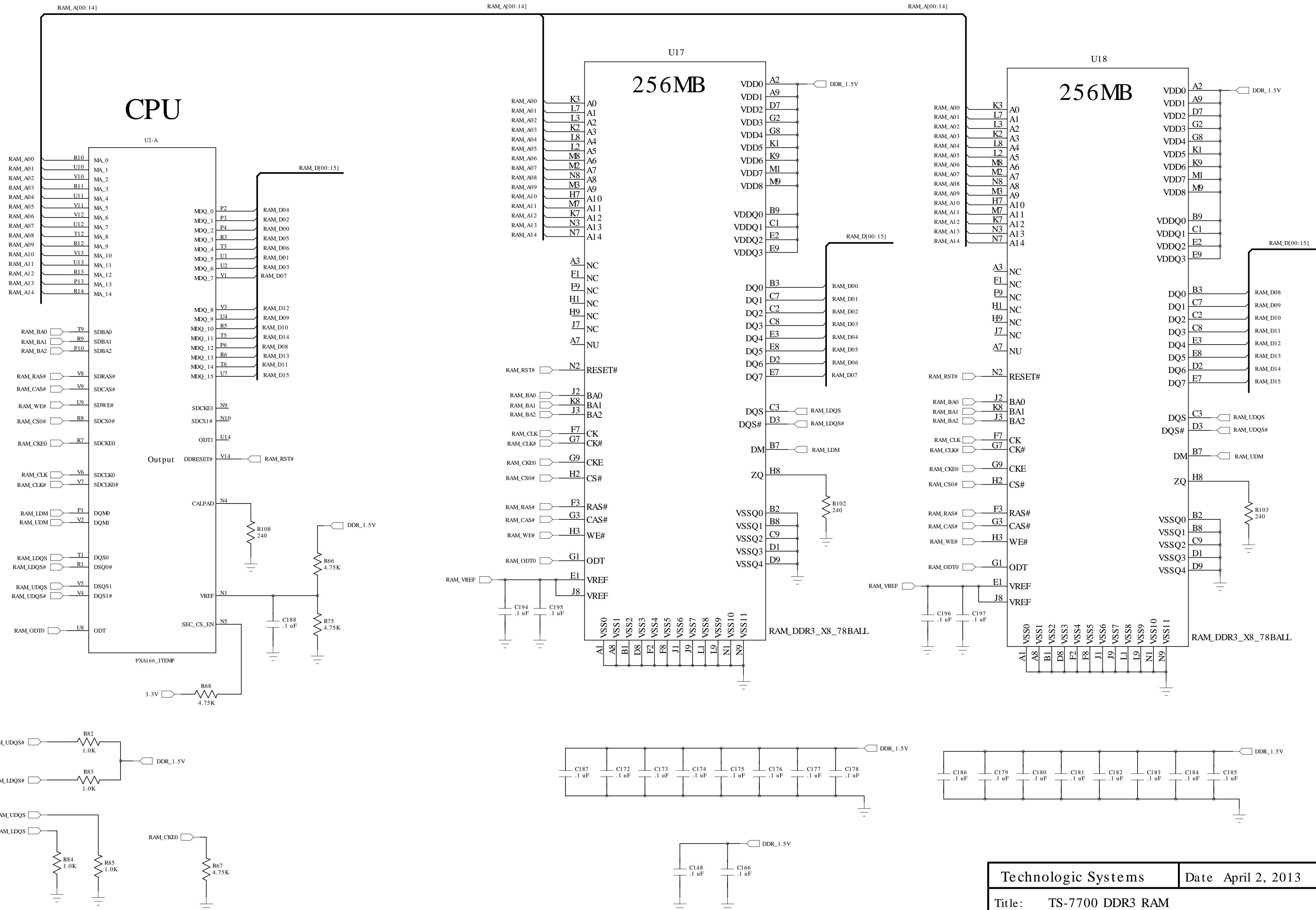
Camera



DDR3 x8 RAM

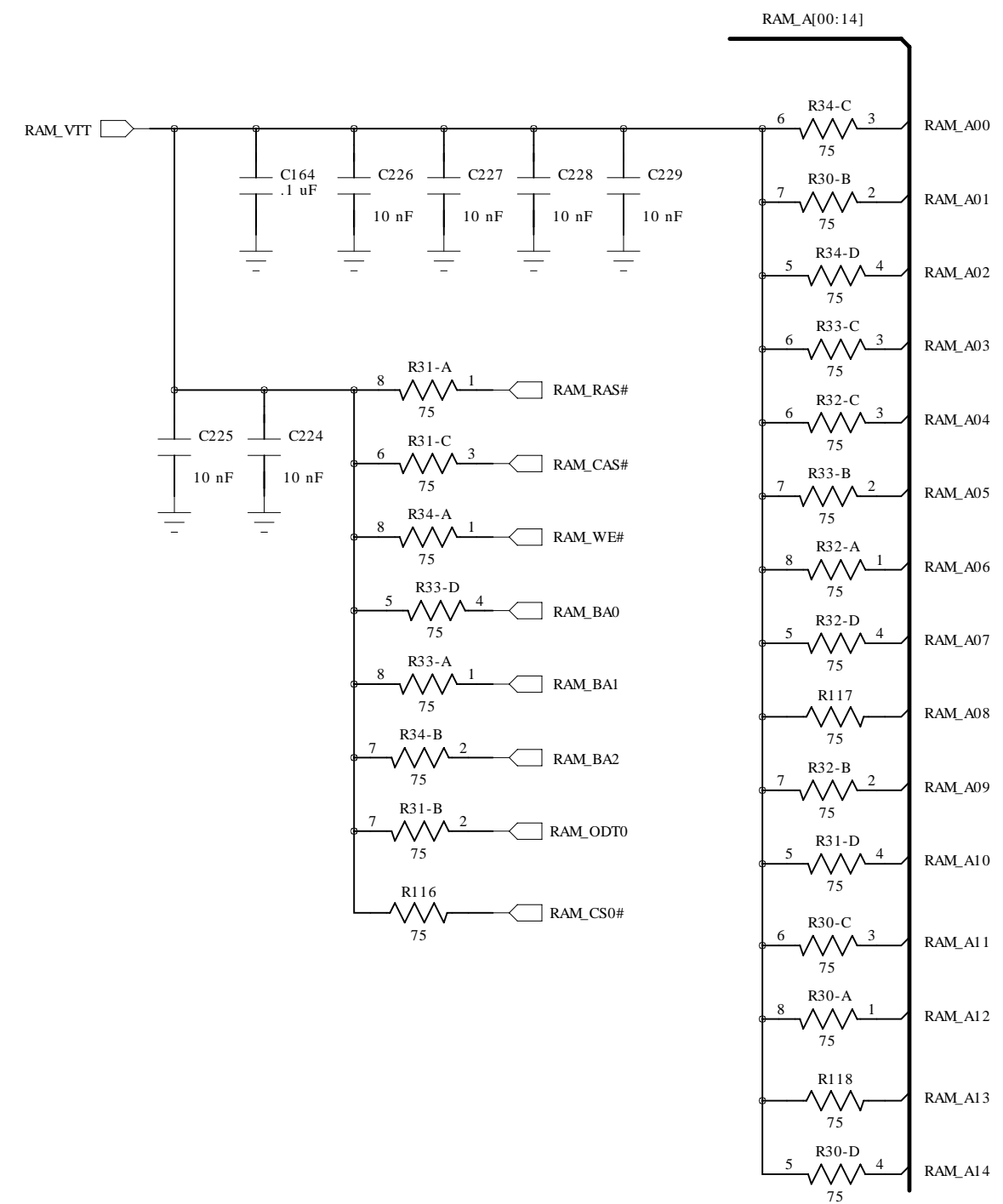
2 Gbit RAM chips

512 MB RAM Total

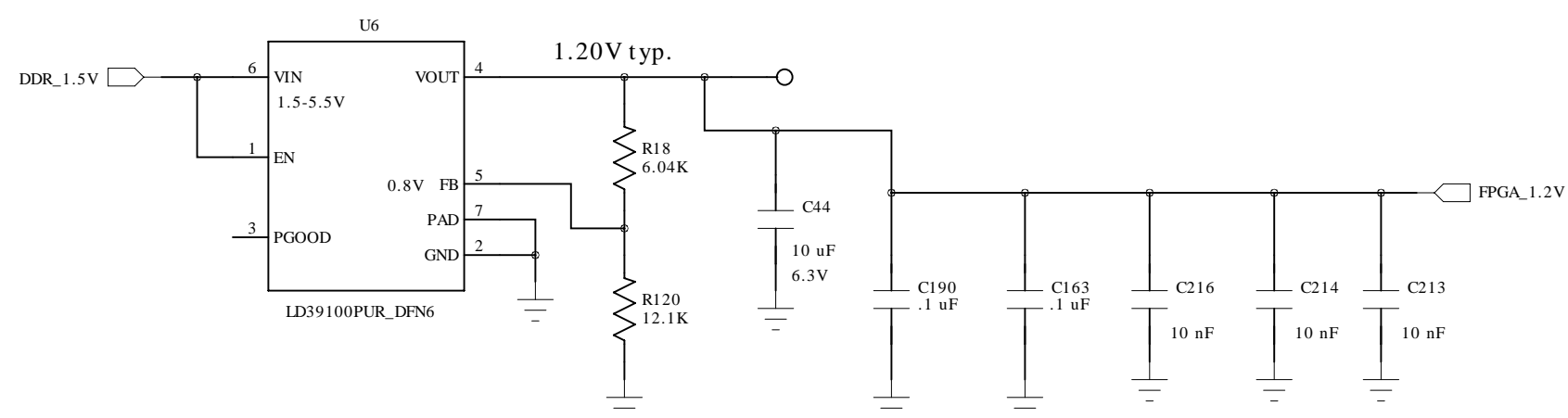


Technologic Systems	Date April 2, 2013
Title: TS-7700 DDR3 RAM	
Rev: A	Designer
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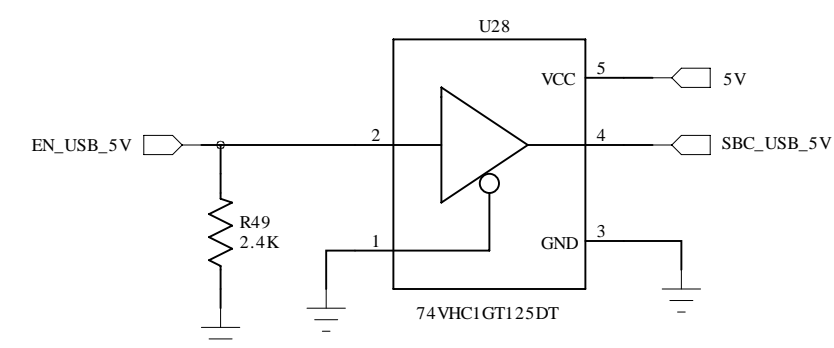
Termination Resistors



FPGA 1.2V Reg.



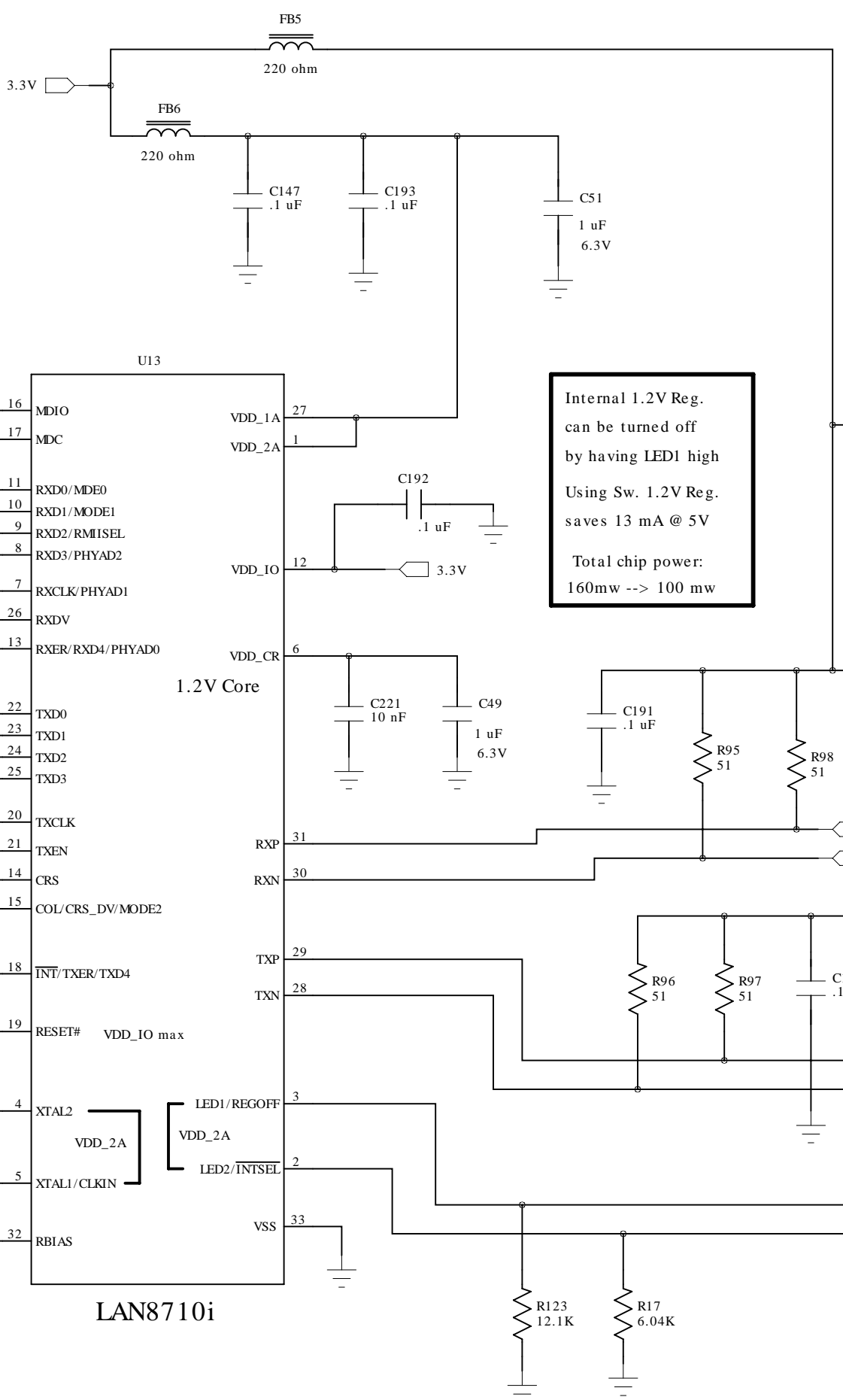
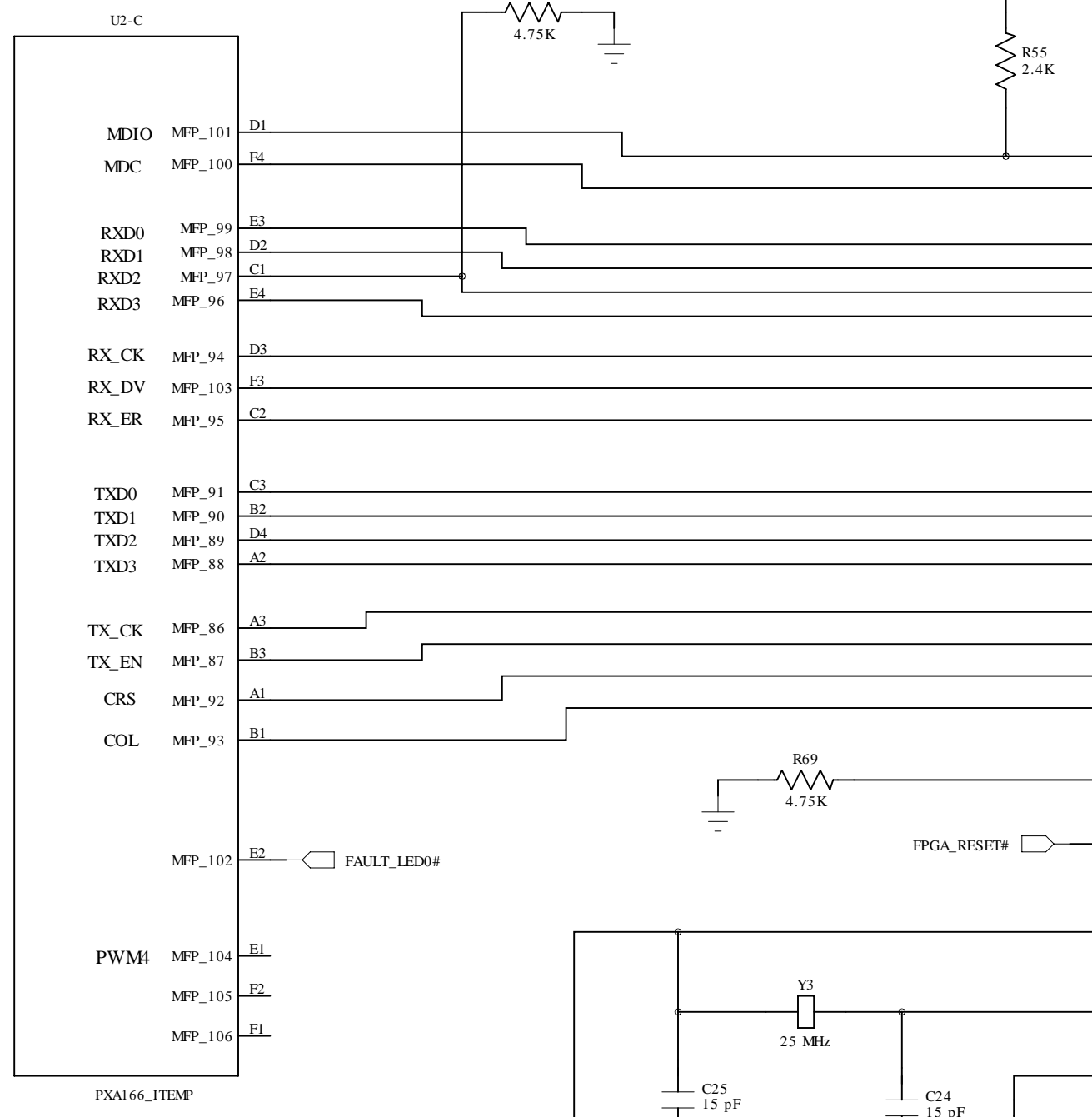
3.3V --> 5V Level Shifter



Technologic Systems	Date April 2, 2013
Title: TS-7700 DDR3 RAM	
Rev: A	Designer
Sheet 3 of 9	

10/100 Ethernet

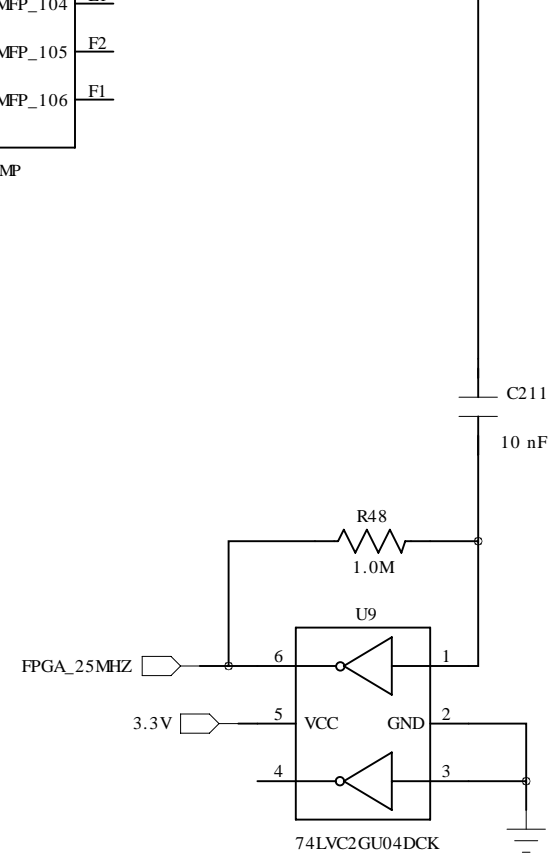
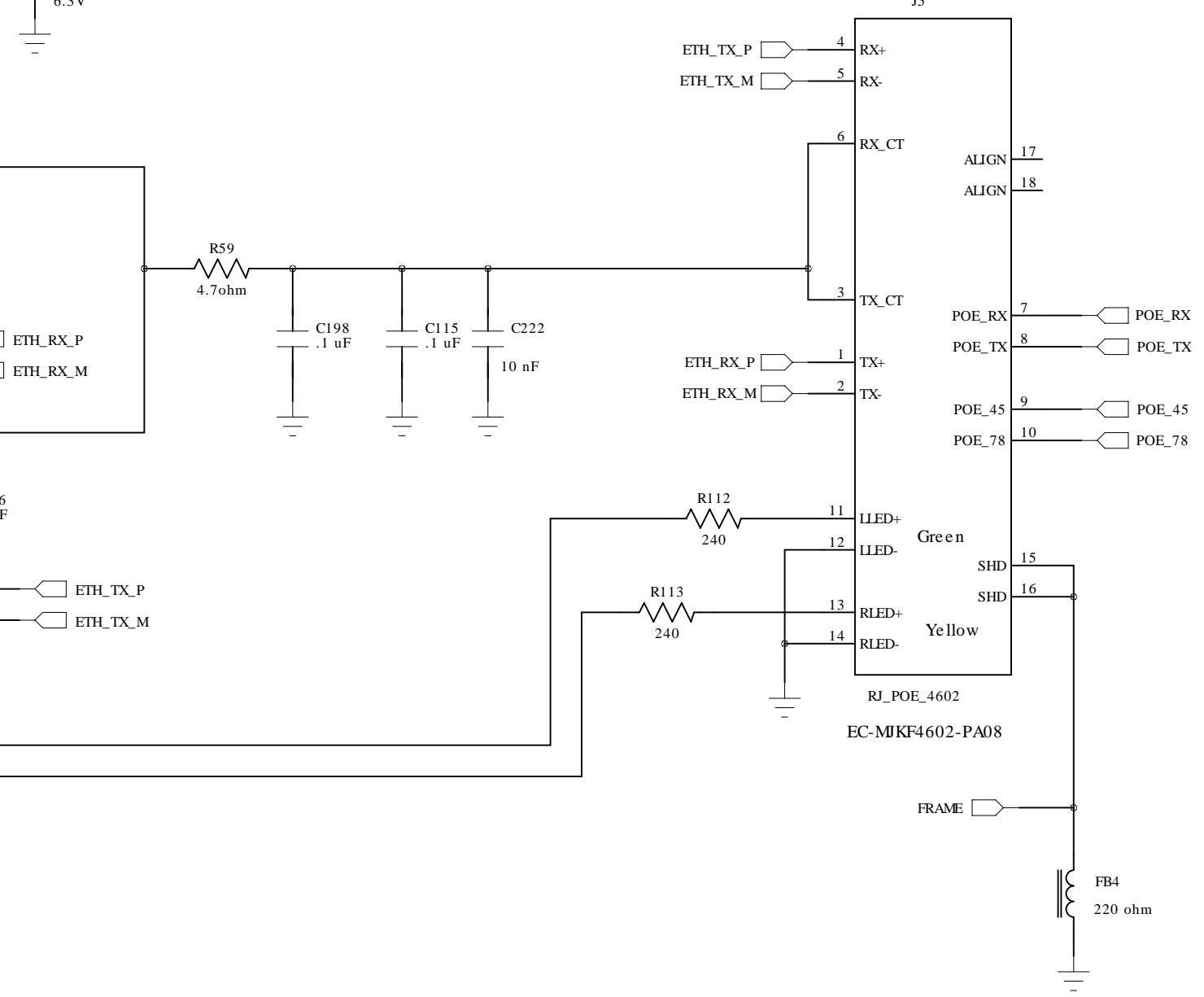
CPU



LAN8710 can power sequence in any order

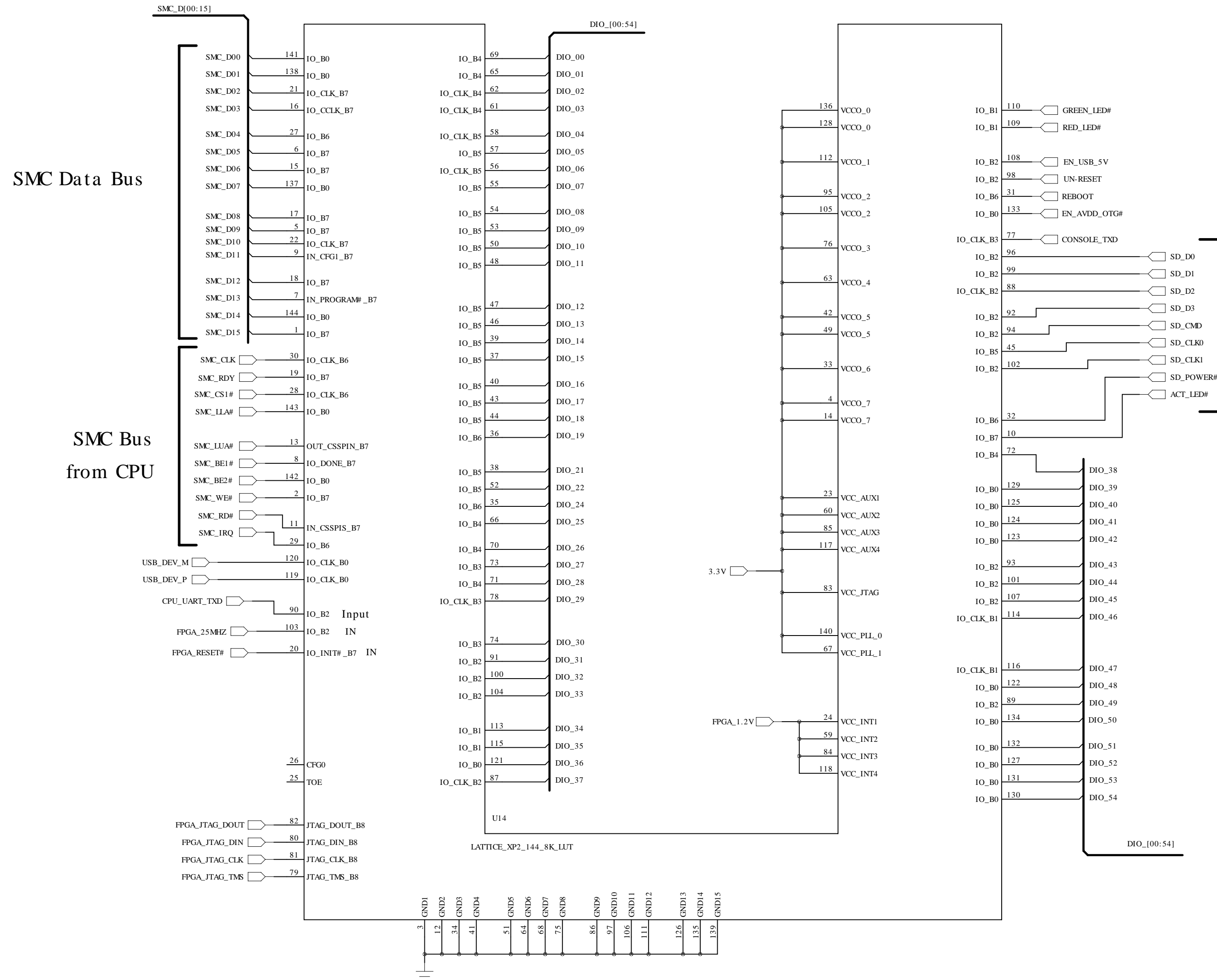
Internal 1.2V Reg. can be turned off by having LED1 high
Using Sw. 1.2V Reg. saves 13 mA @ 5V
Total chip power: 160mw --> 100 mw

10/100 Ethernet

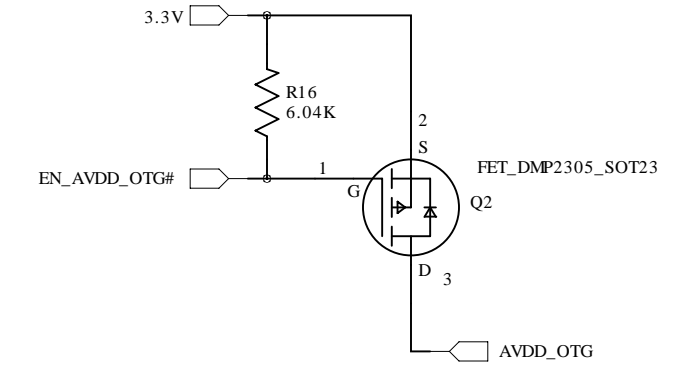


Technologic Systems	Date April 2, 2013
Title: TS-7700 Ethernet PHY	
Rev: A	Designer RLM Sheet 4 of 9

FPGA with 8000 LUTs



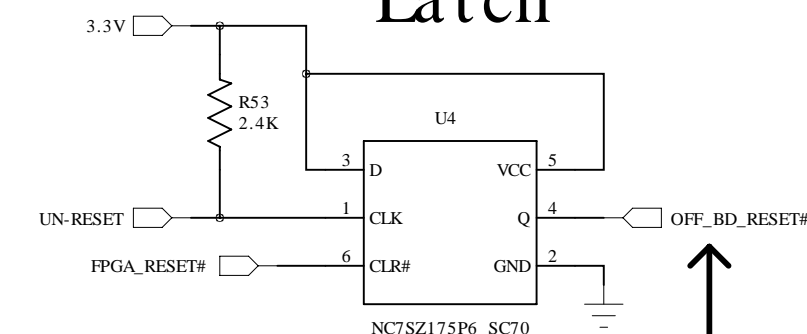
CPU USB Power



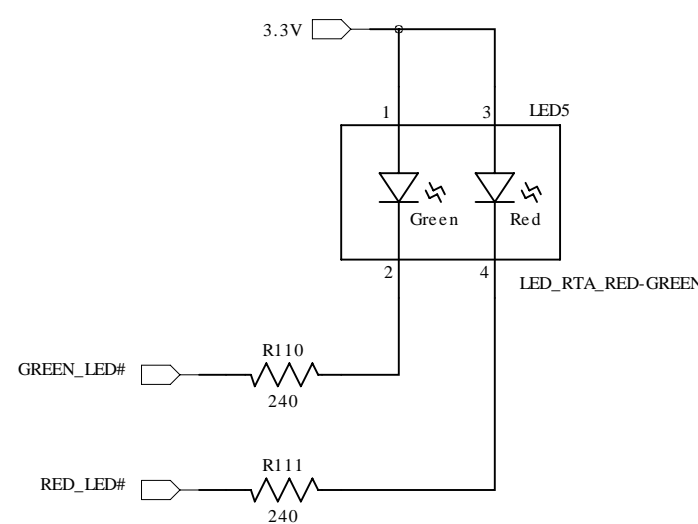
After FPGA_RESET# is deasserted
Assert EN_AVDD_OTG#
Then wait another 10-20 mS
before "Un-resetting" CPU

SD Cards

Reset Latch



This drives CPU_RESET#



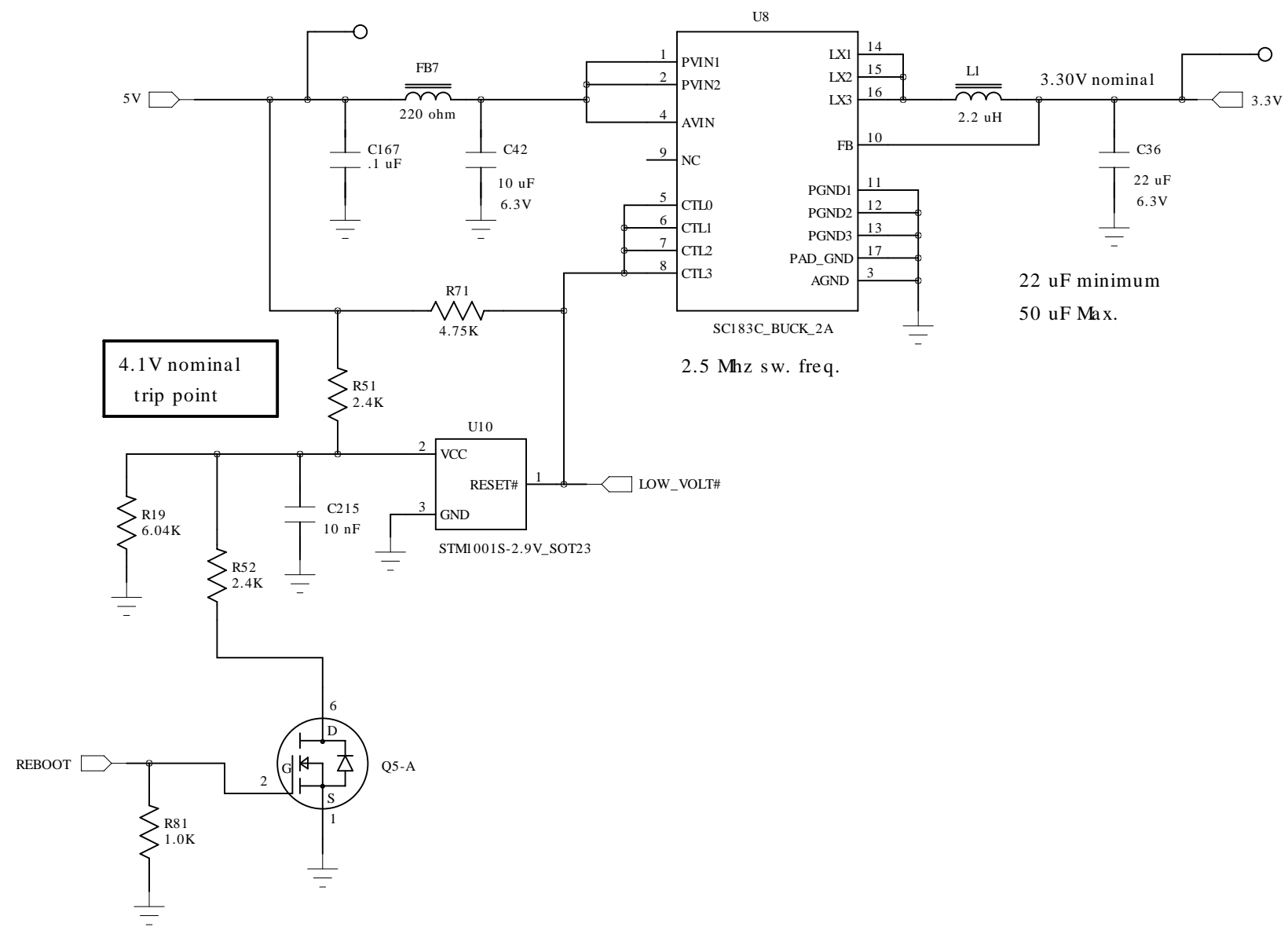
XP2-5 has:
5K or 8K LUTs 2 PLLs
9/12 blocks of 1Kx18 Block RAM
12 18x18 Multipliers
100 I/O with 144 pin package
"instant ON" = about 1.5 mS
input PLL clock = 10 MHz min

Pull-up and pull-down resistors
are 6 to 30K ohms

Page 37 of Data Sheet (Hot Socketing)
Power Supplies can be sequenced in any order
but must be monotonic
All I/O lines are tri-stated during power cycling

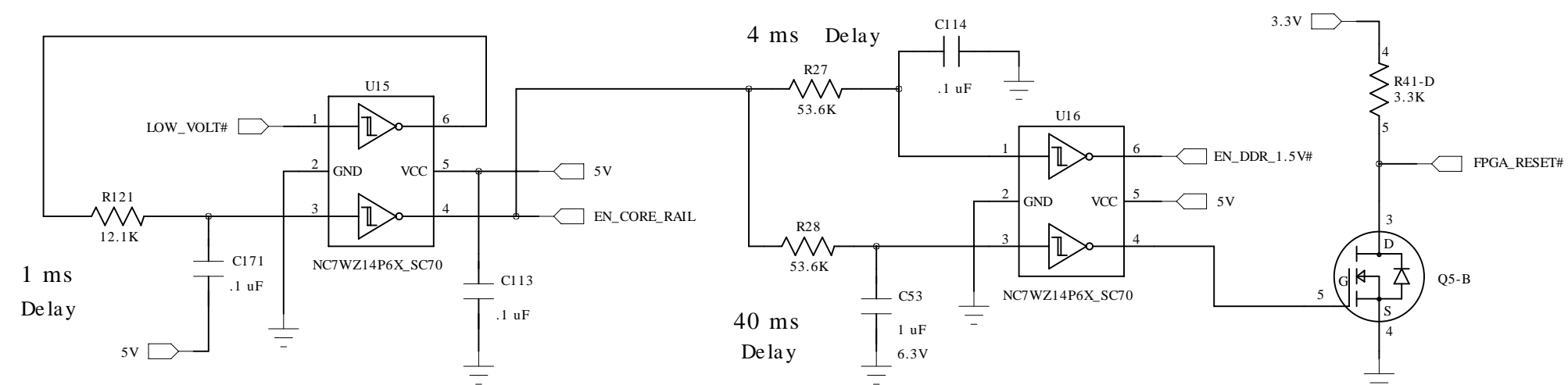
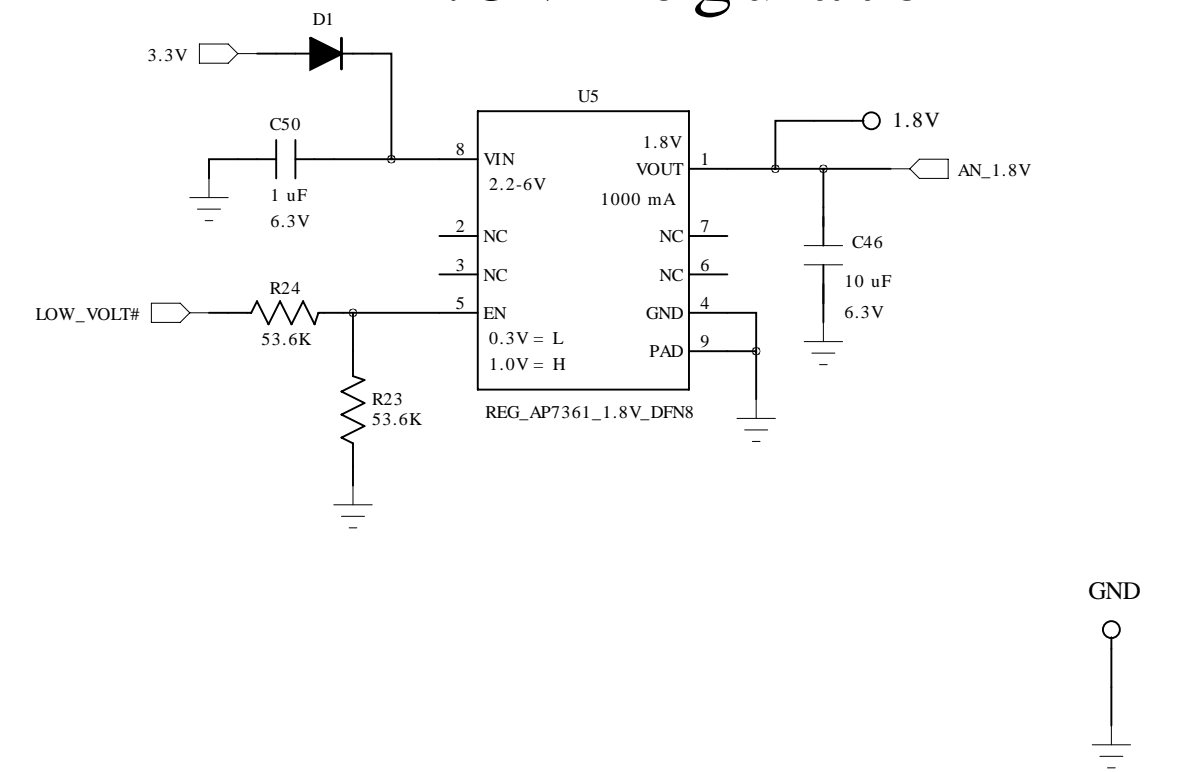
3.3V Power Supply

up to 2000 mA

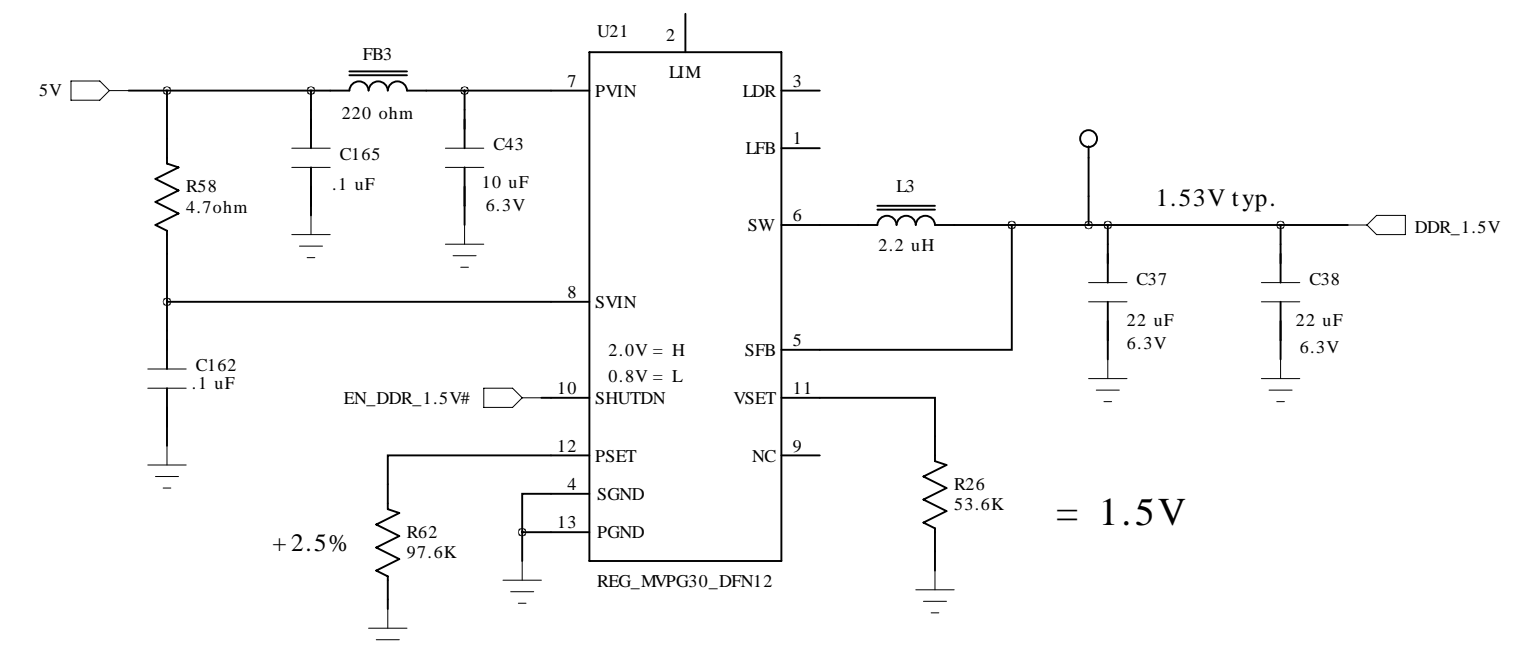


Power Supplies

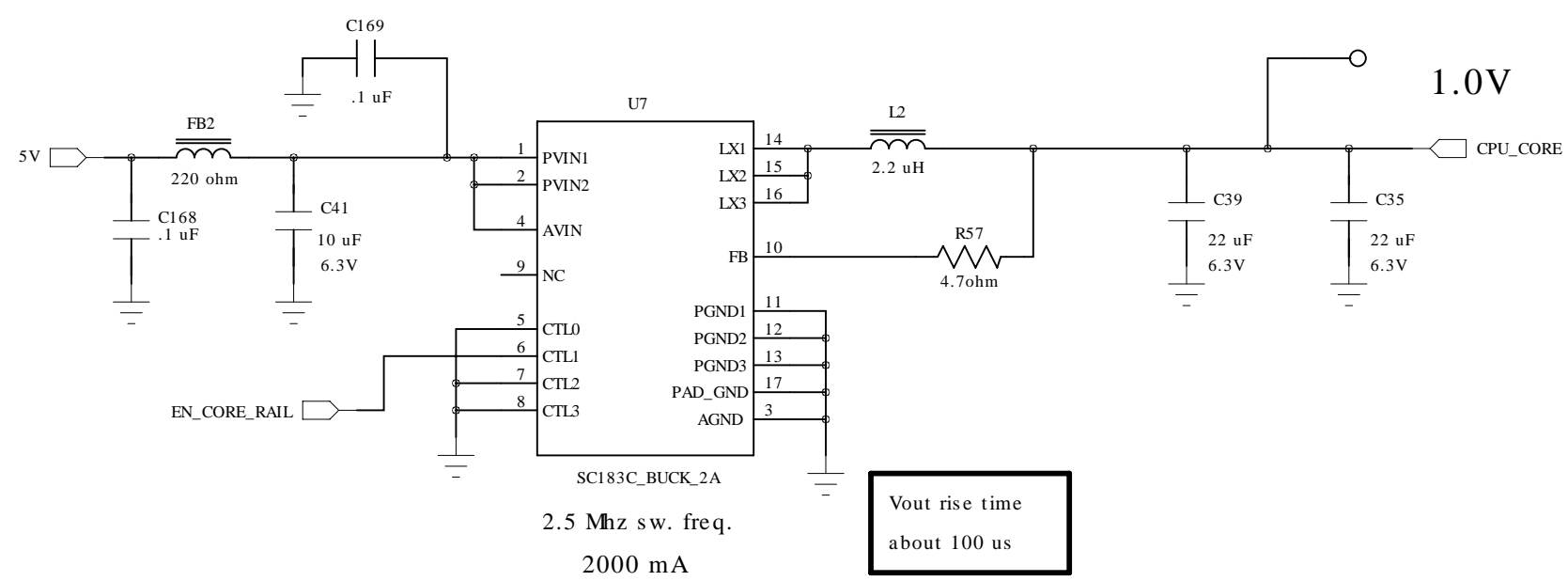
Analog 1.8V Regulator



DDR3 1.5V Reg.

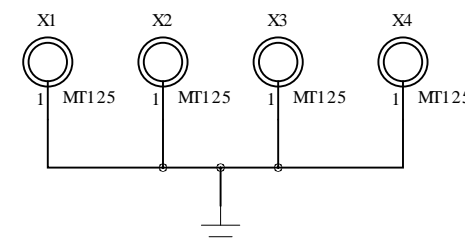
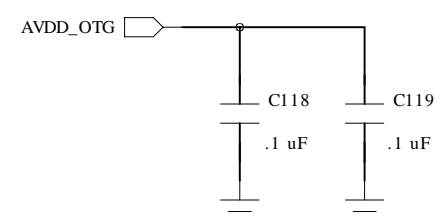
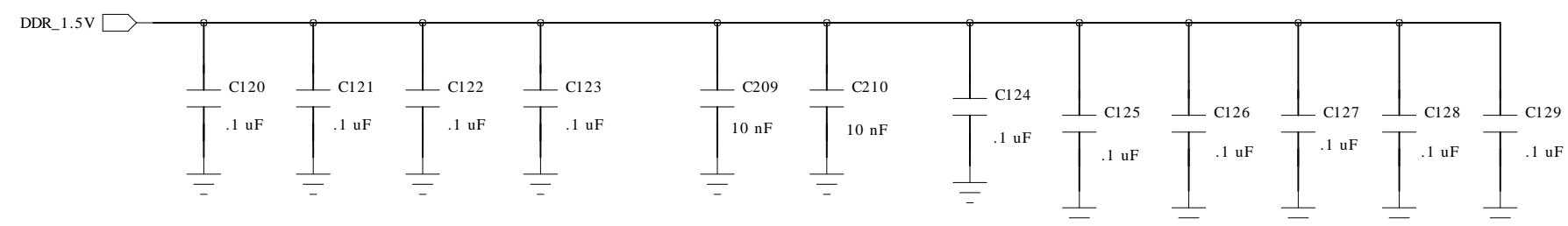
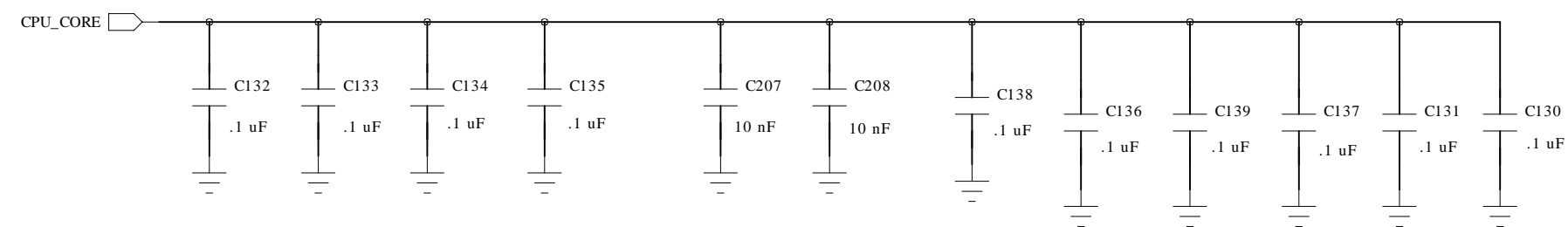
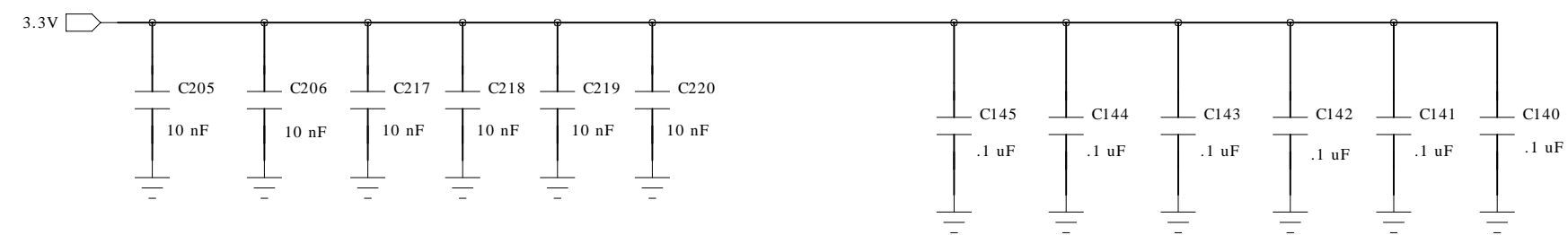
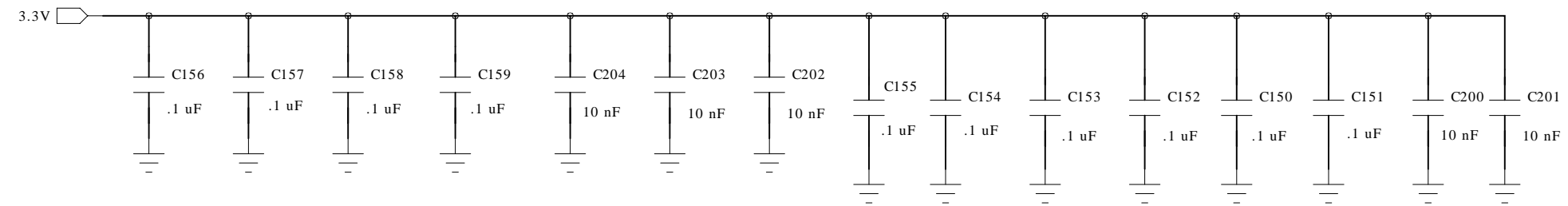


CPU Core Supply



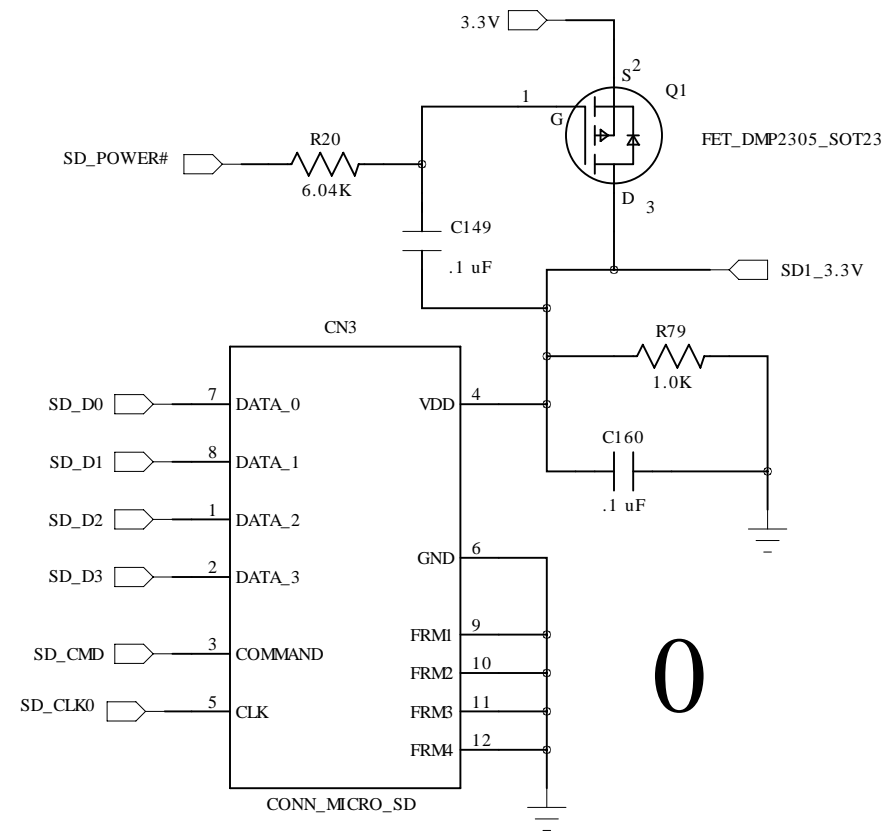
Technologic Systems	Date April 2, 2013
Title: TS-7700 Power Supplies	
Rev: A	Designer
Sheet 6 of 9	

CPU Power

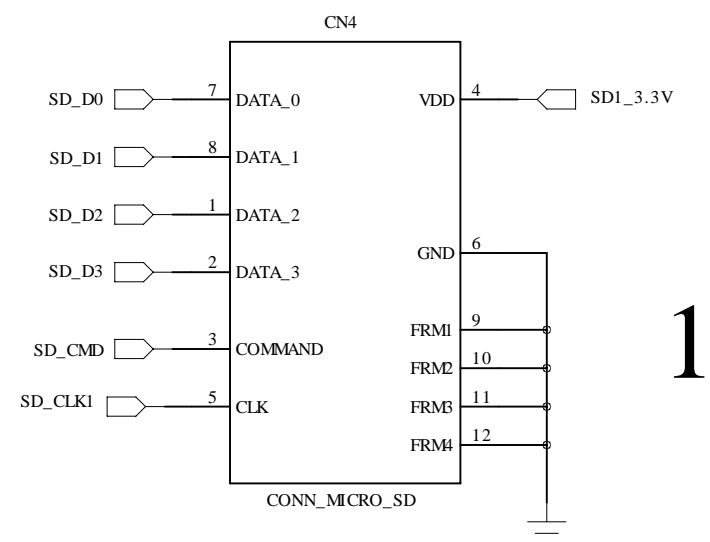


Technologic Systems		Date April 2, 2013
Title: TS-7700 CPU Power and Bypass caps		
Rev: A	Designer	Sheet 7 of 9

Micro SD Card Sockets

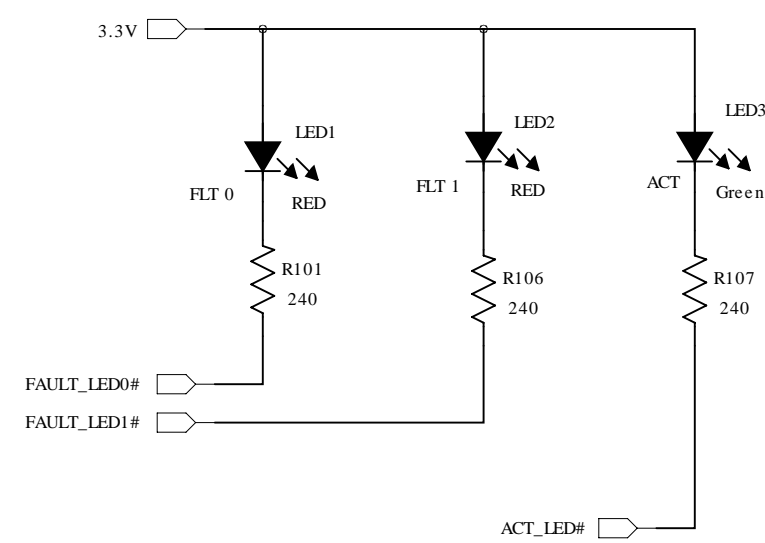


0

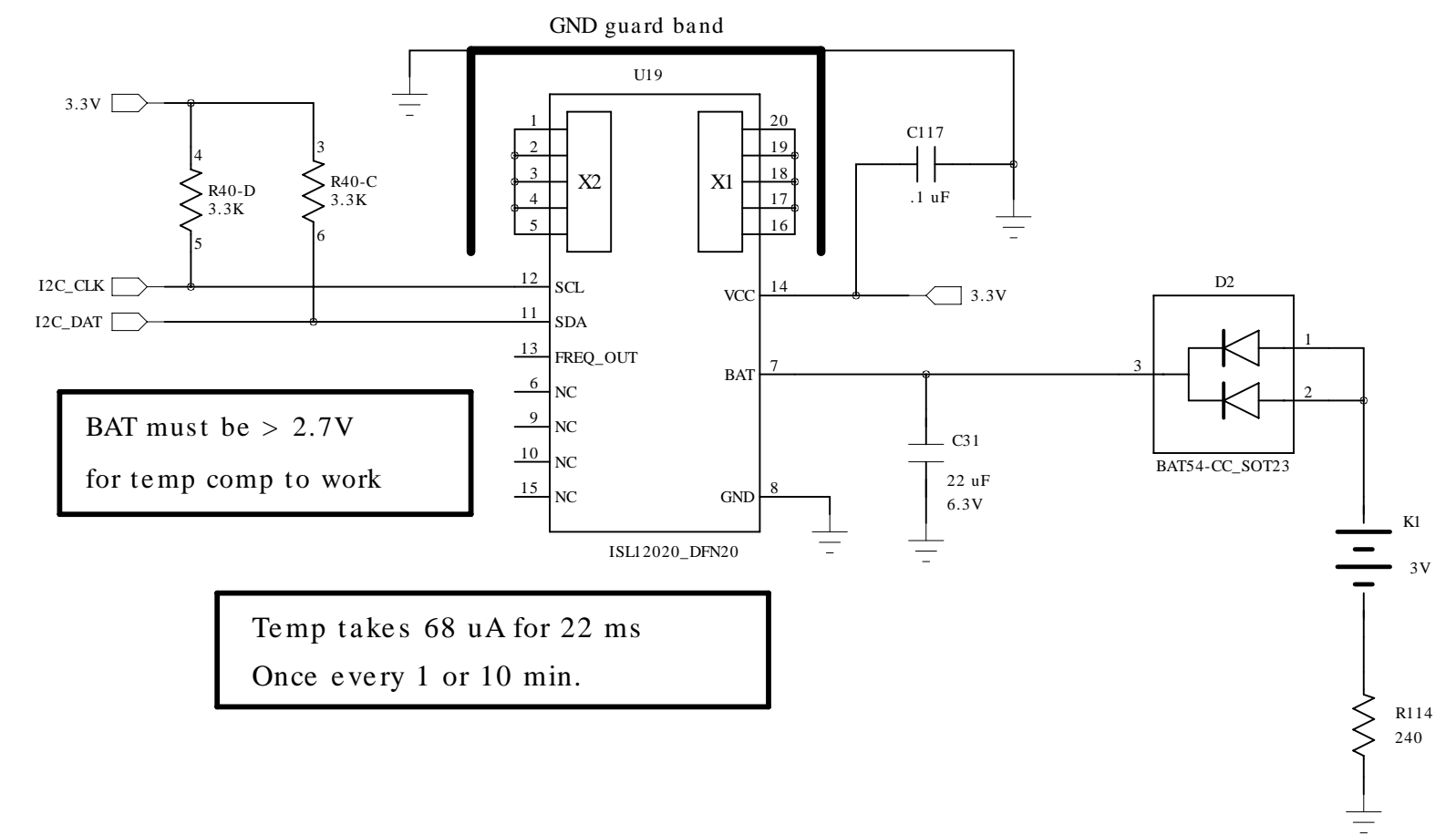


1

SD Card LEDs



RTC and Temp. Sensor

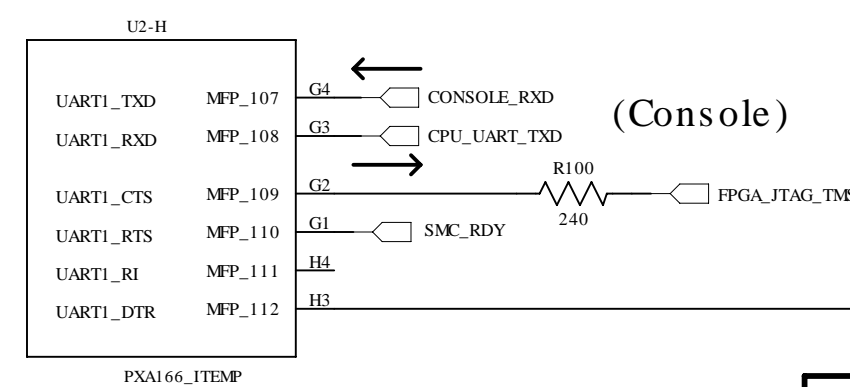


BAT must be > 2.7V
for temp comp to work

Temp takes 68 uA for 22 ms
Once every 1 or 10 min.

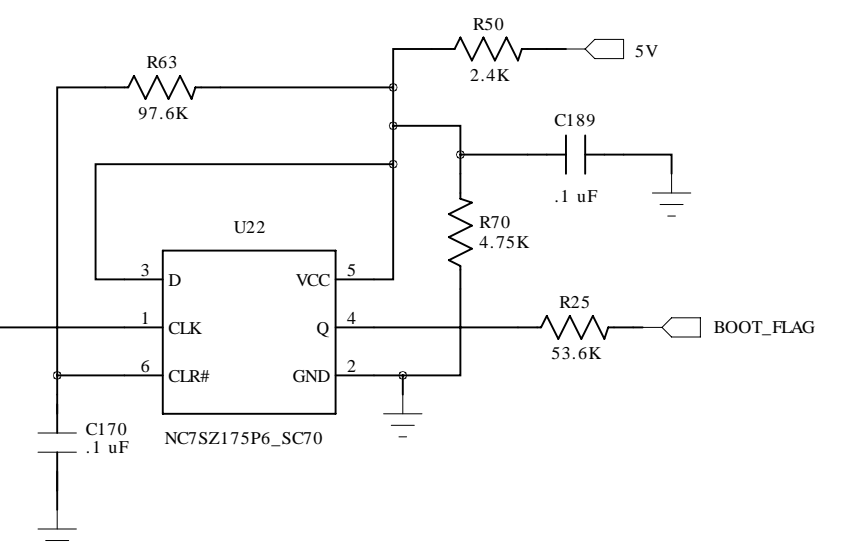
CPU

Debug UART

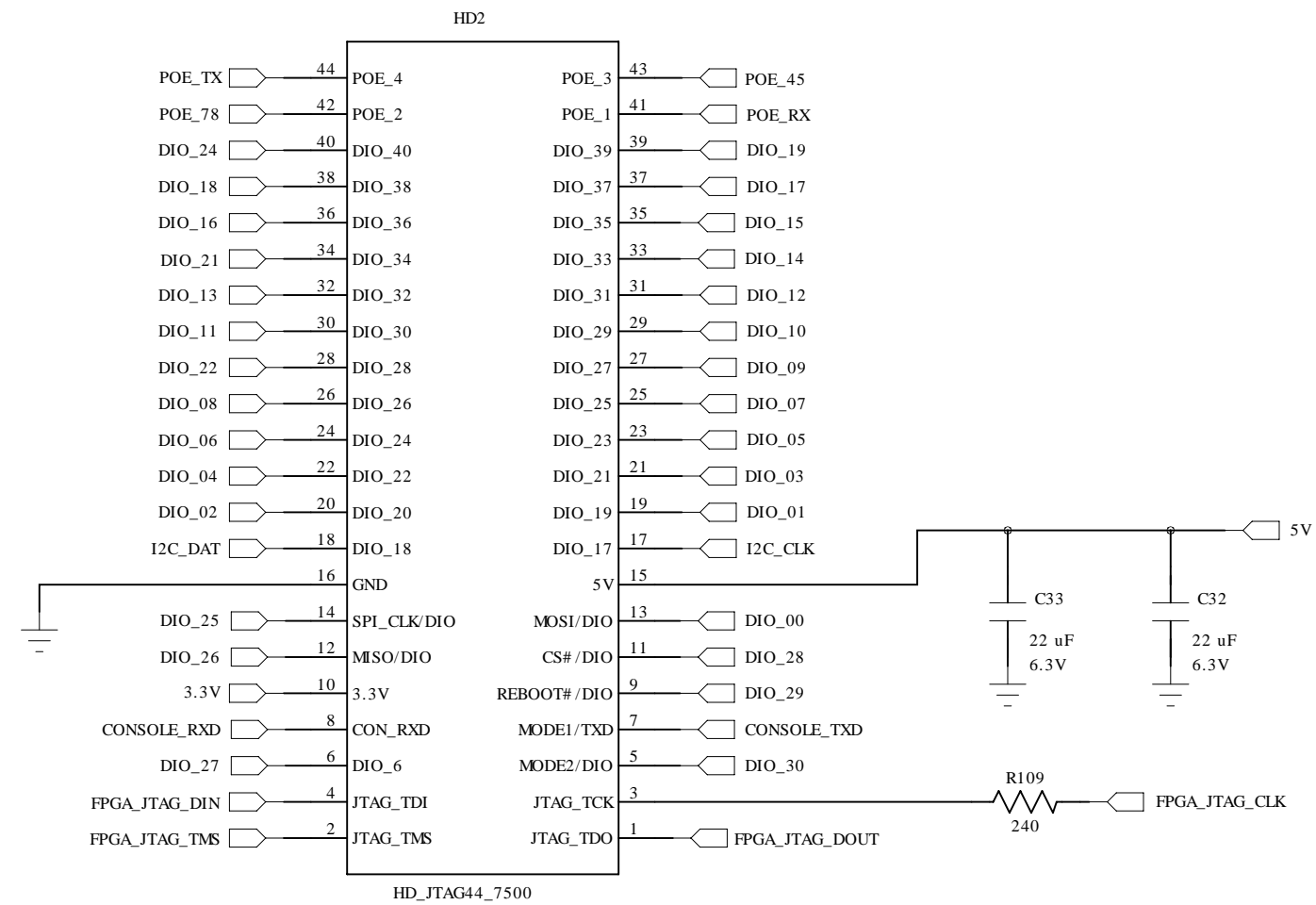


Keep normally
at logic zero

Reboot Flag



44-Pin DIO Header



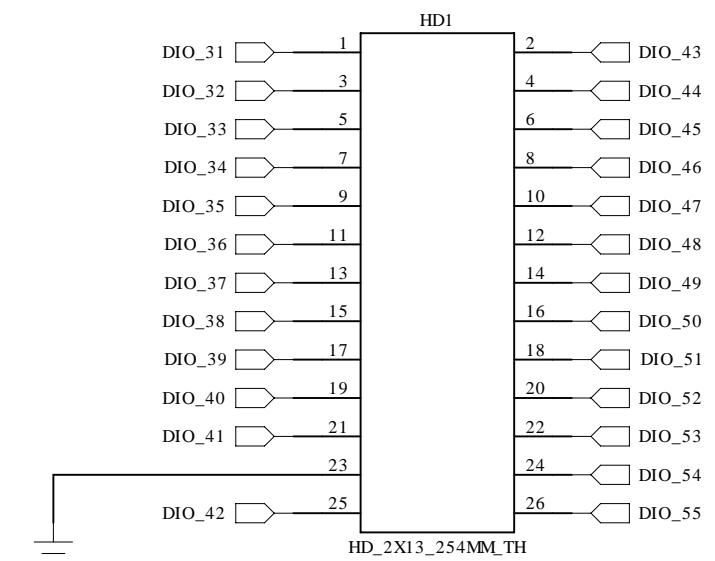
MODE1 and MODE2 states are latched when CPU_RESET# is deasserted

Logic "0" on MODE2 signal forces Boot from SD card

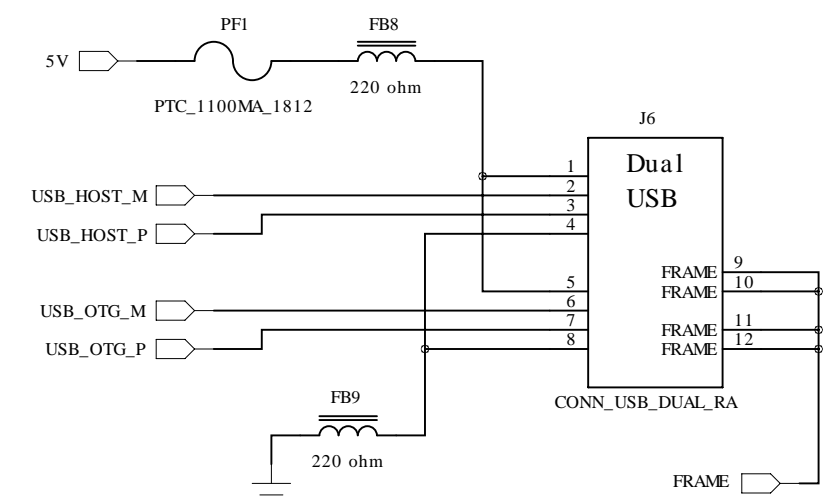
MODE1 and MODE2 have 4.7K resistor pull-ups on TS-7500

Logic "0" on MODE1 forces Console onto the TXD and RXD lines

26-Pin DIO Header



USB Host Ports



USB Device Port

