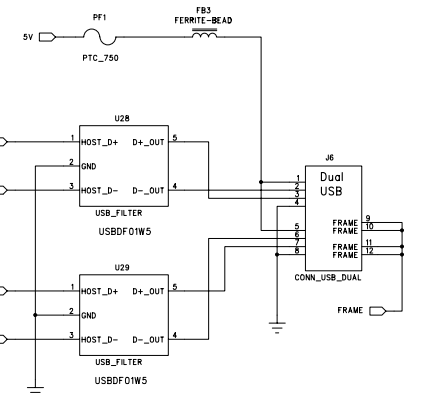
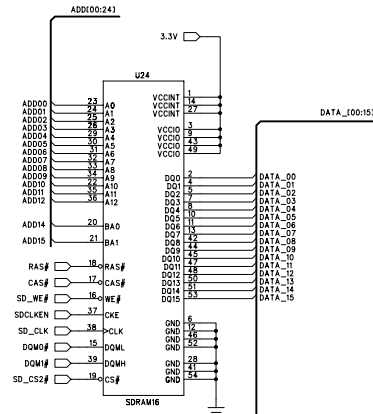


USB Ports

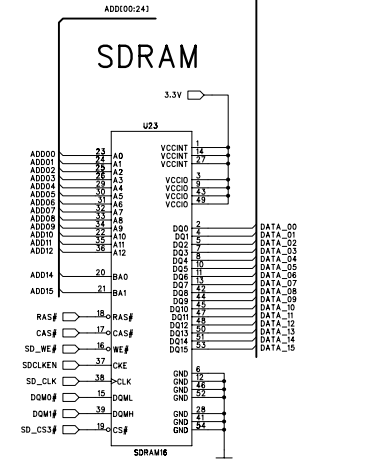


Technologic Systems	Date March 17, 2008
Title: TS-7370 EP9302 CPU, USB	
Rev:	Designer RLM Sheet 1 of 7

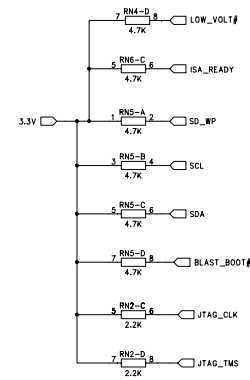
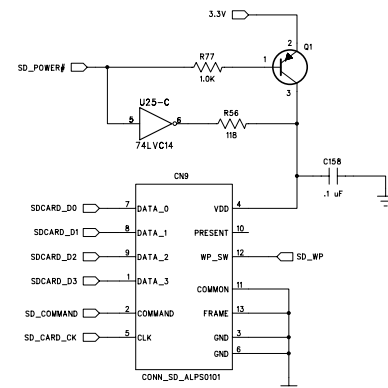
SDRAM



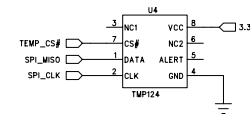
SDRAM



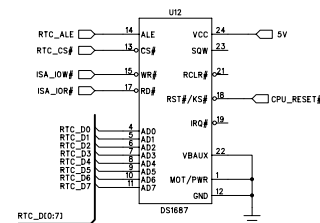
SD Card Socket



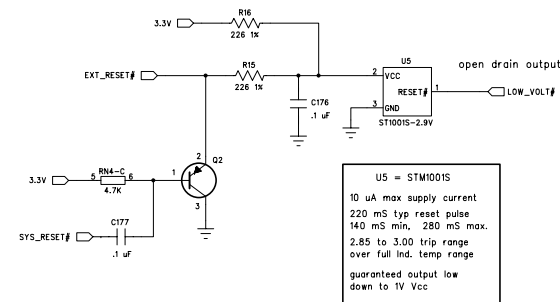
Temp Sensor



Battery-Backed Real Time Clock



Power On Reset

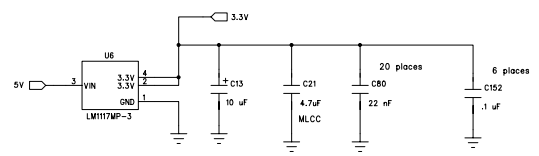


U5 = ST100IS
 10 uA max supply current
 220 mS typ reset pulse
 140 mS min, 280 mS max.
 2.85 to 3.00 trip range
 over full ind. temp range
 guaranteed output low
 down to 1V Vcc

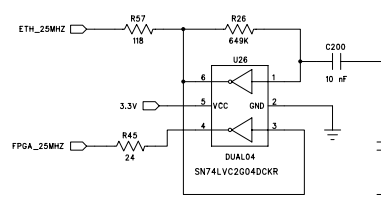
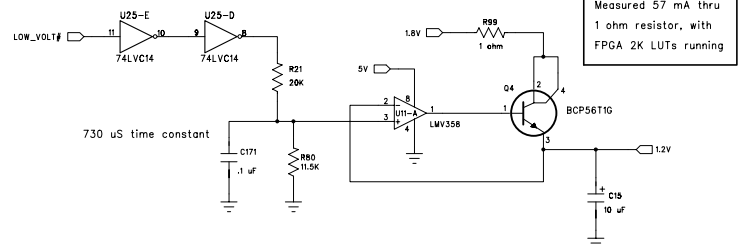


Technologic Systems	Date March 17, 2008
Title: TS-7370 SDRAM, Flash, RTC, POR	
Rev:	Designer RLM Sheet 2 of 7

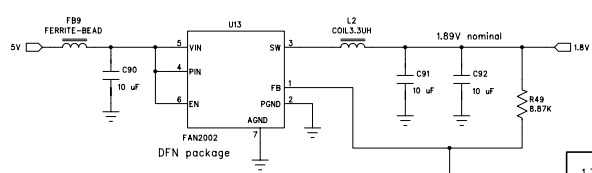
3.3V Regulator



1.2V Regulator



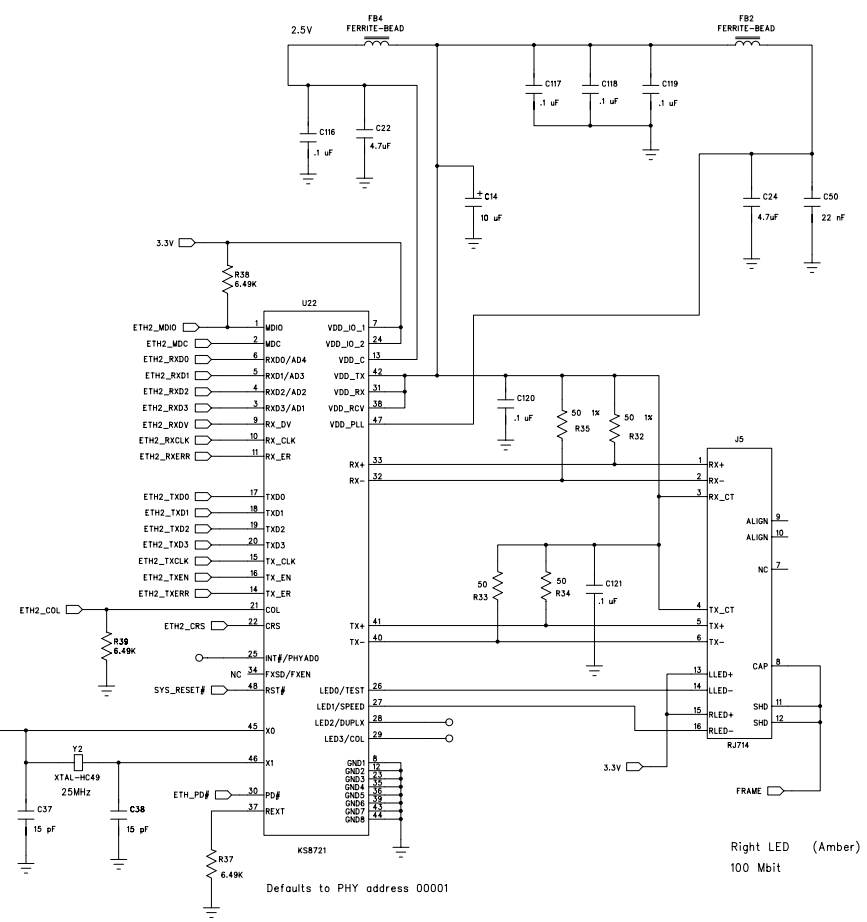
1.8V Switching Regulator



FAN2002

1.3 MHz freq. 50 uA quiescent
 Vout = 800mV * [1+ Rtop/Rbot]
 > 90% eff. at 100-400 mA load
 1000 mA max load

10/100 Ethernet

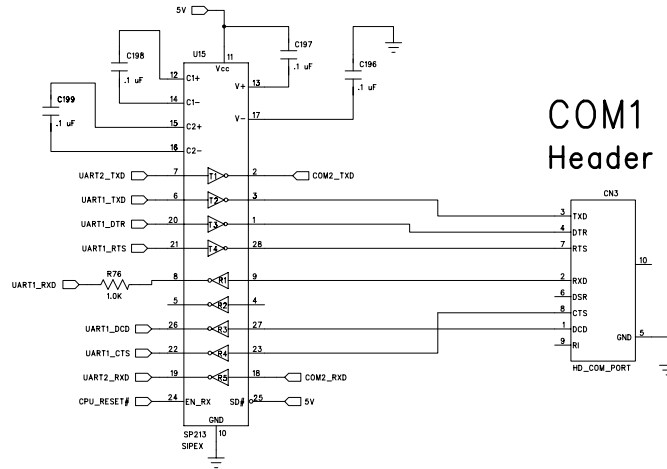


Right LED (Amber)
100 Mbit

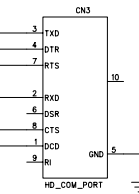
Left LED (Green)
Link / Activity

Technologic Systems	Date March 17, 2008
Title: TS-7370 Power Supplies, Ethernet	
Rev:	Designer RLM Sheet 3 of 7

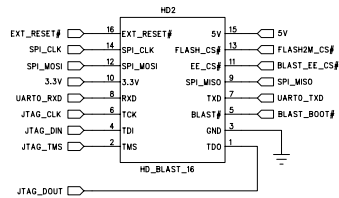
RS-232 Transceiver



COM1 Header



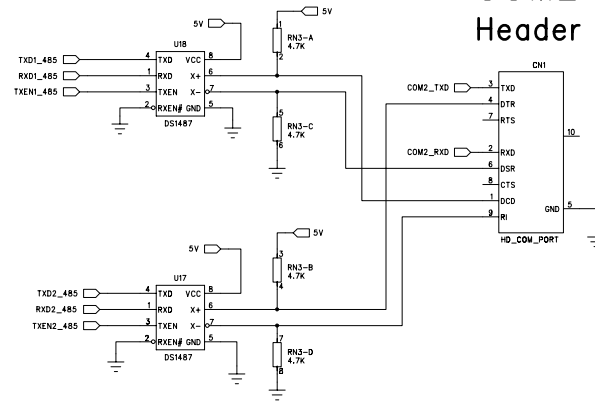
JTAG Header



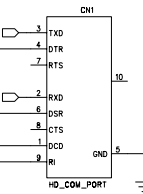
BLAST_EE_CS# is not used for booting -- FPGA Boot code has capability to boot from 2MB Serial Flash directly

Logic "0" on "BLAST_BOOT#" signal indicates Boot using TS-9444 2MB Flash

RS-485 Drivers



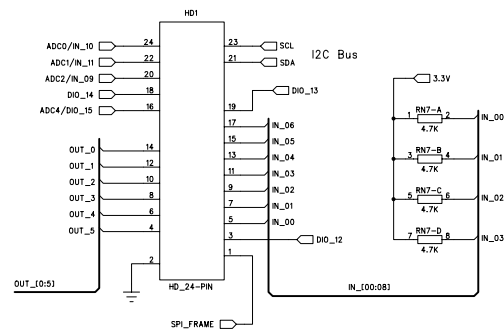
COM2 Header



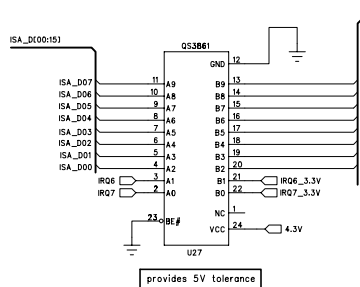
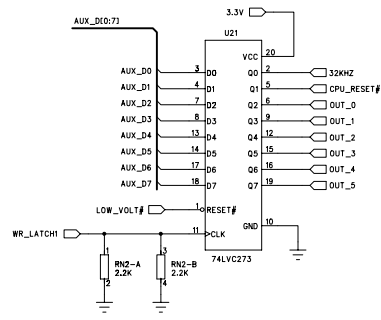
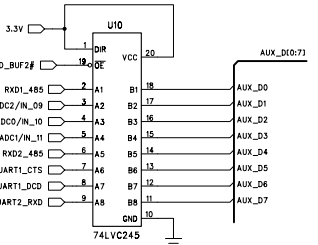
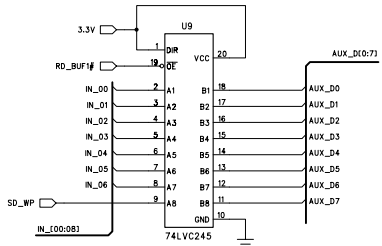
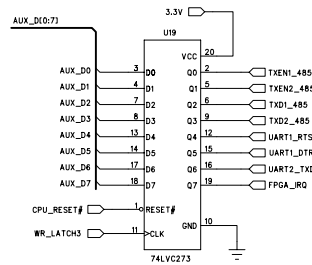
24-pin Header

24 + 16 = 40-pin Header

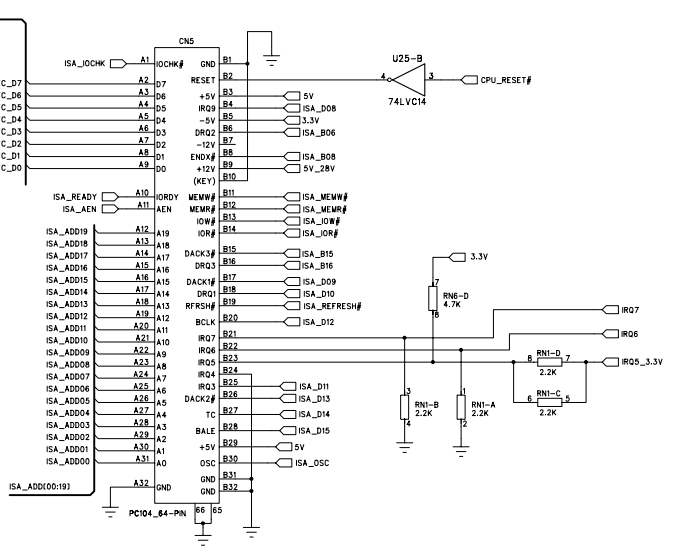
- 4 ADC
- ADC lines in parallel with IN_09, IN_10, IN11, DIO15
- 2 I2C
- 1 GND
- 6 Latched Outputs (OUT0-OUT5)
- 7 Buffered Inputs (IN0-IN6)
- 3 DIO_12, DIO_13, DIO_14
- 1 SPI_FRAME



Technologic Systems	Date	March 17, 2008
Title: TS-7370	COM Ports	DIO JTAG Headers
Rev:	Designer	Sheet 4 of 7

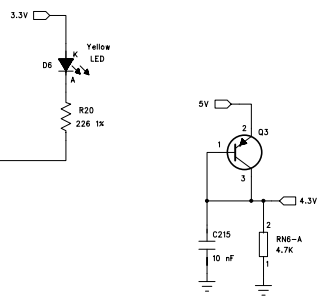
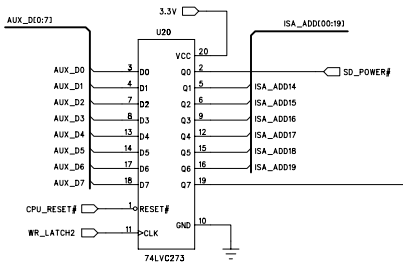


PC/104 64-pin Connector



Warning:
 All IRQs and data lines DO-D7 are 5V tolerant
 all other signals must use 3.3V levels
 IRQ3 must be 3.3V levels

33 lines directly into FPGA
 plus 10 more (D0-D7 and IOR, IOW)
 that can be used with no RTC option
 plus 6 more from latch (A14-A19)



Technologic Systems		Date March 17, 2008
Title: TS-7370 PC/104 AUX Bus		
Rev:	Designer	Sheet 6 of 7

