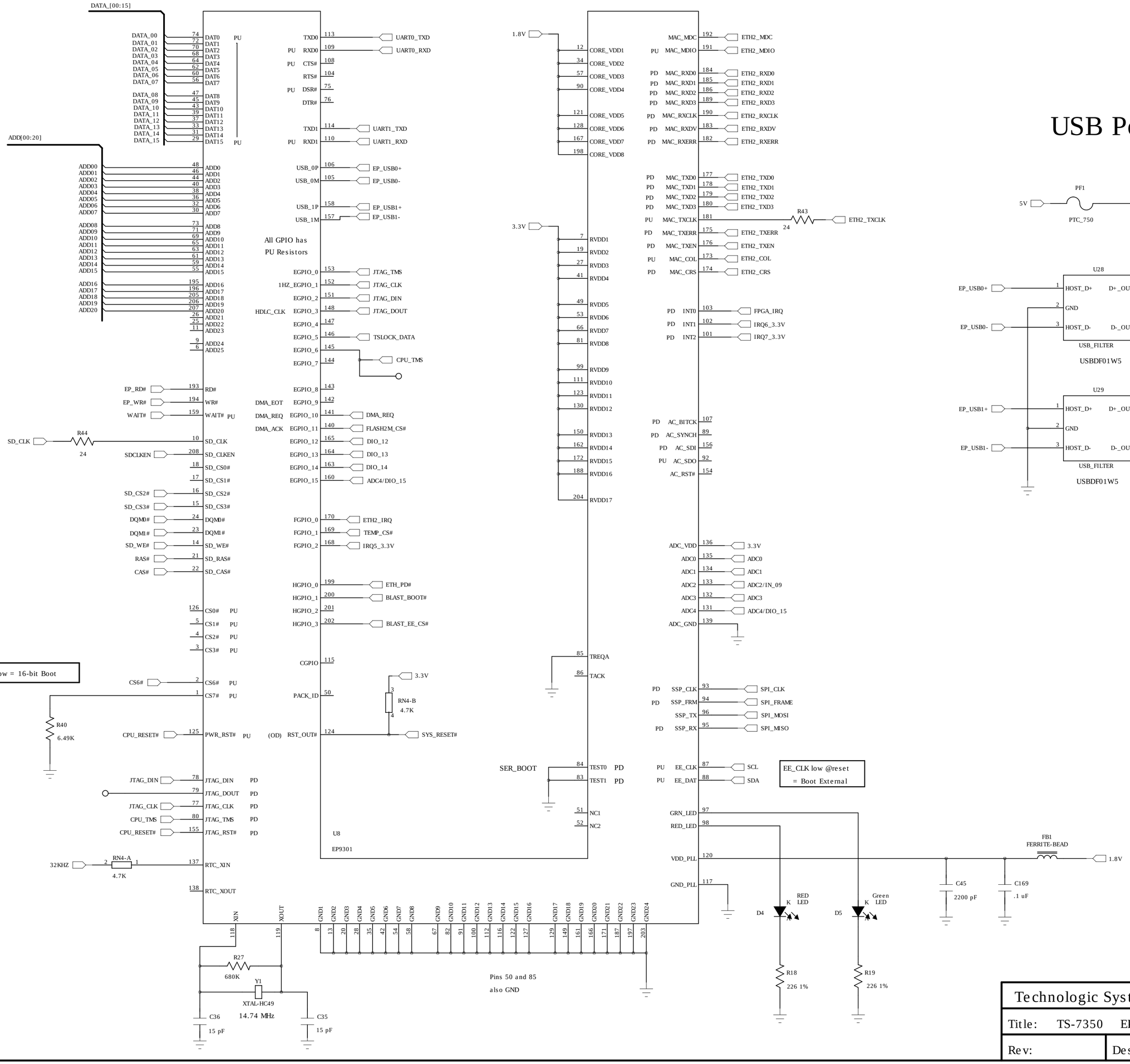
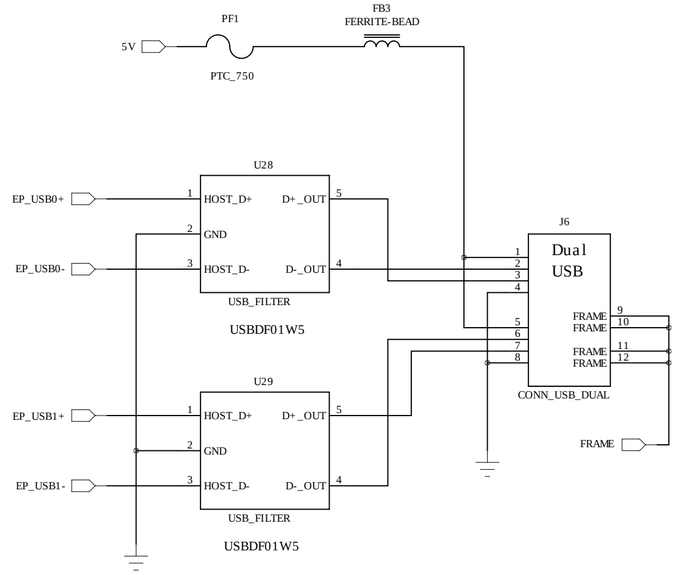
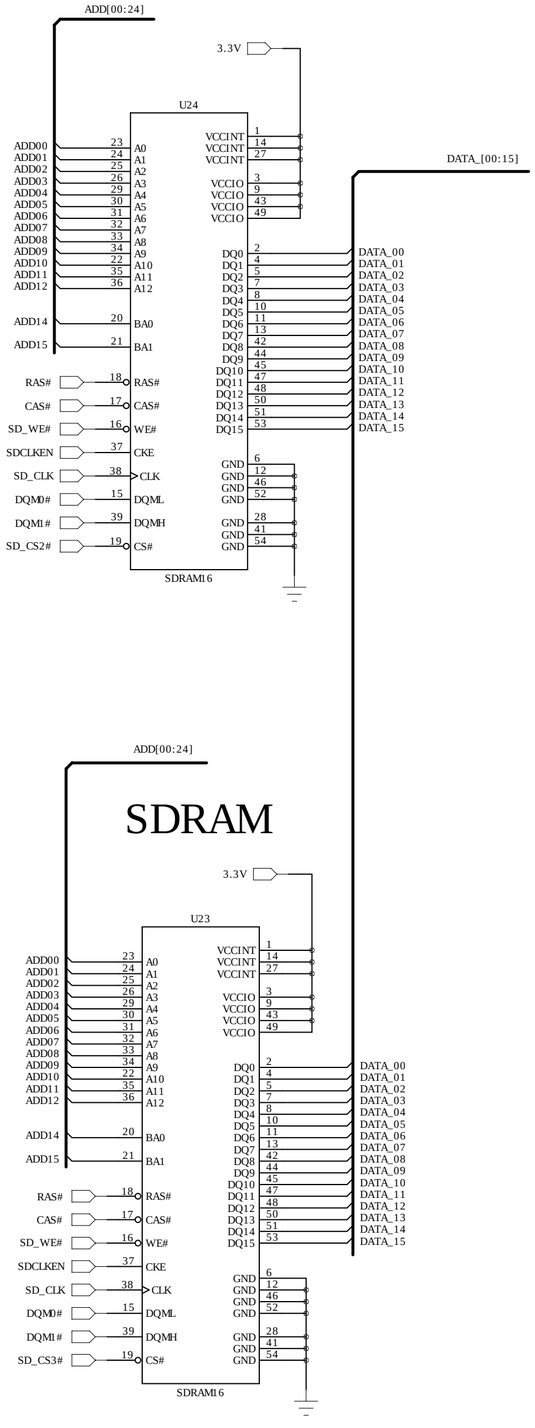


USB Ports

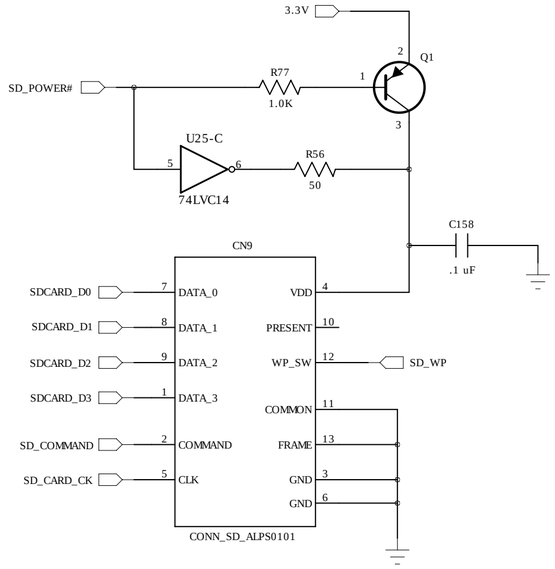


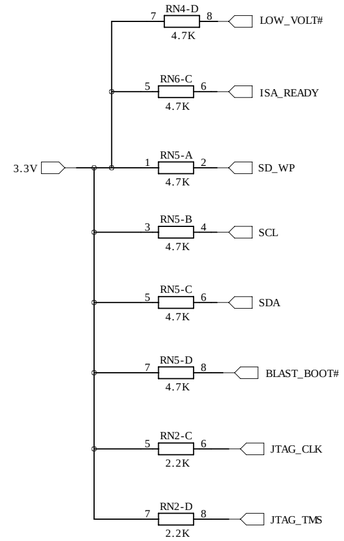
Technologic Systems	Date March 15, 2008	
Title: TS-7350 EP9302 CPU, USB		
Rev:	Designer RLM	Sheet 1 of 7

SDRAM

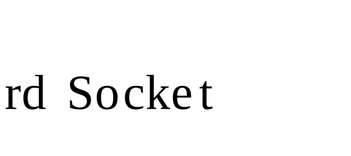


SD Card Socket

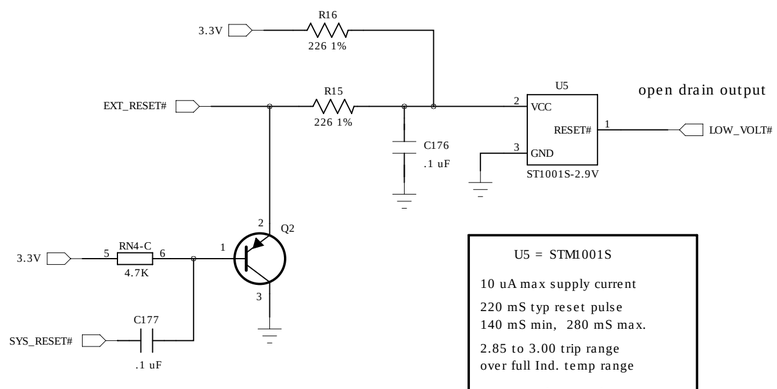




Temp Sensor



Power On Reset



U5 = STM1001S

10 uA max supply current

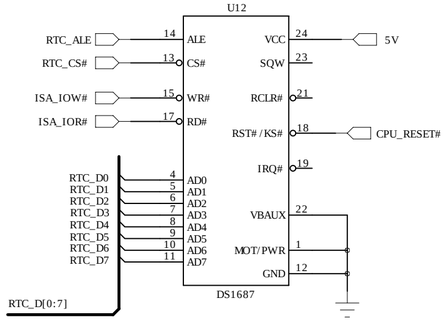
220 mS typ reset pulse
140 mS min, 280 mS max.

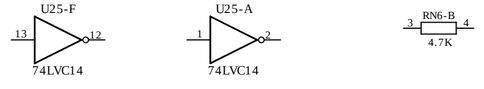
2.85 to 3.00 trip range
over full Ind. temp range

guaranteed output low
down to 1V Vcc

but can only sink 1.2 mA

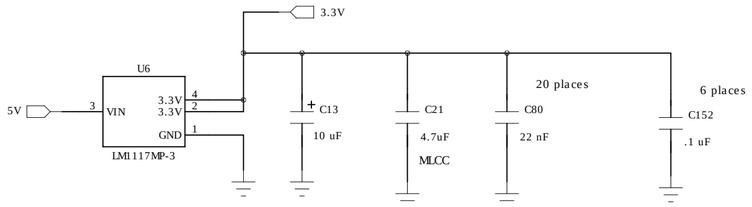
Battery-Backed Real Time Clock





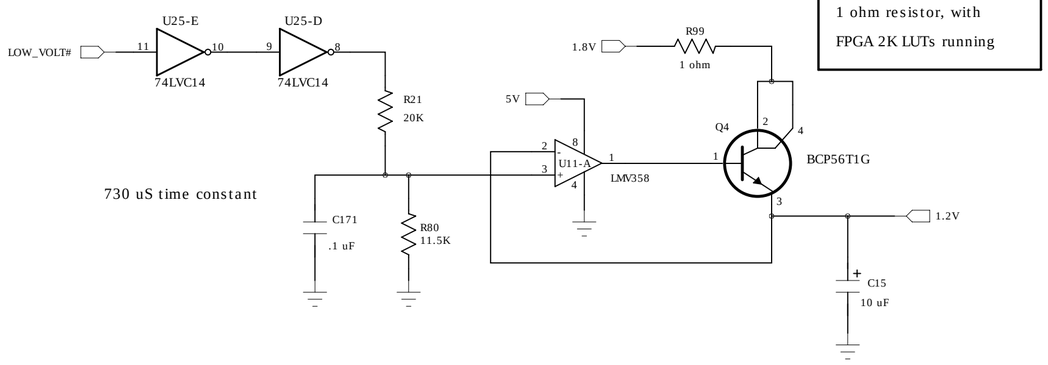
Technologic Systems		Date March 15, 2008
Title: TS-7350 SDRAM, Flash, RTC, POR		
Rev:	Designer RLM	Sheet 2 of 7

3.3V Regulator

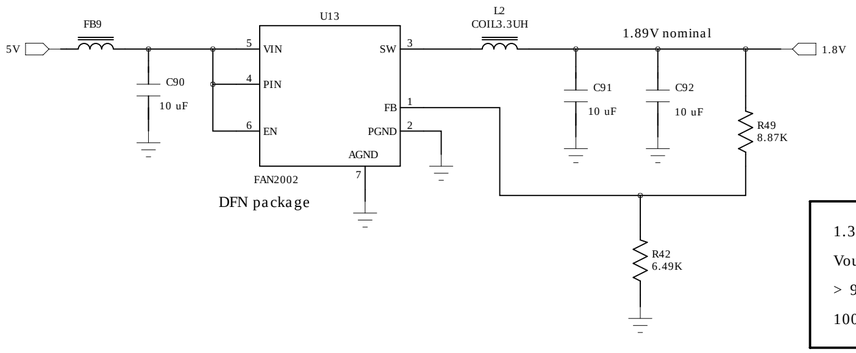


1.2V Regulator

Measured 57 mA thru
1 ohm resistor, with
FPGA 2K LUTs running



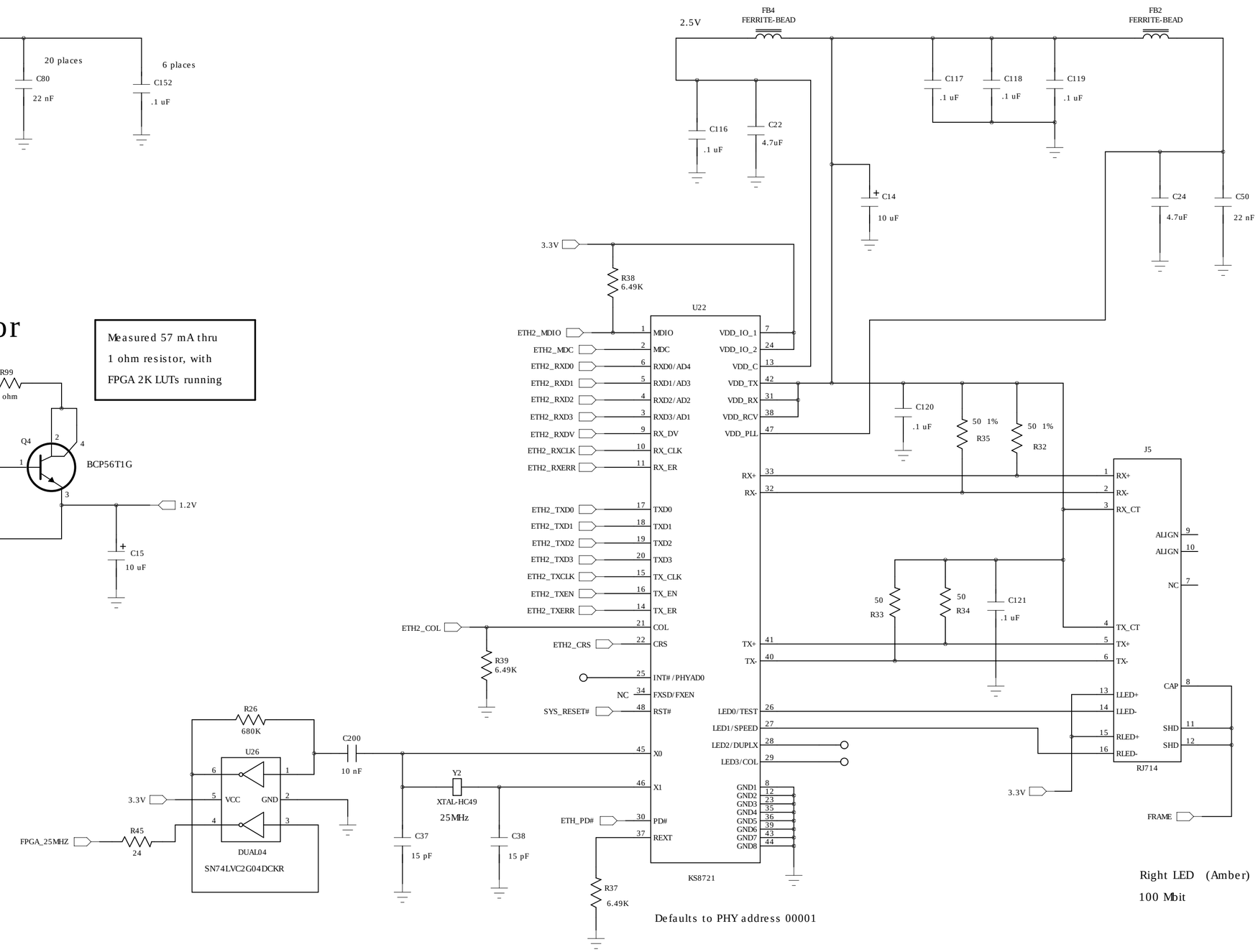
1.8V Switching Regulator



FAN2002

1.3 MHz freq. 50 uA quiescent
Vout = 800mV * [1+ Rtop/Rbot]
> 90% eff. at 100-400 mA load
1000 mA max load

10/100 Ethernet



Defaults to PHY address 00001

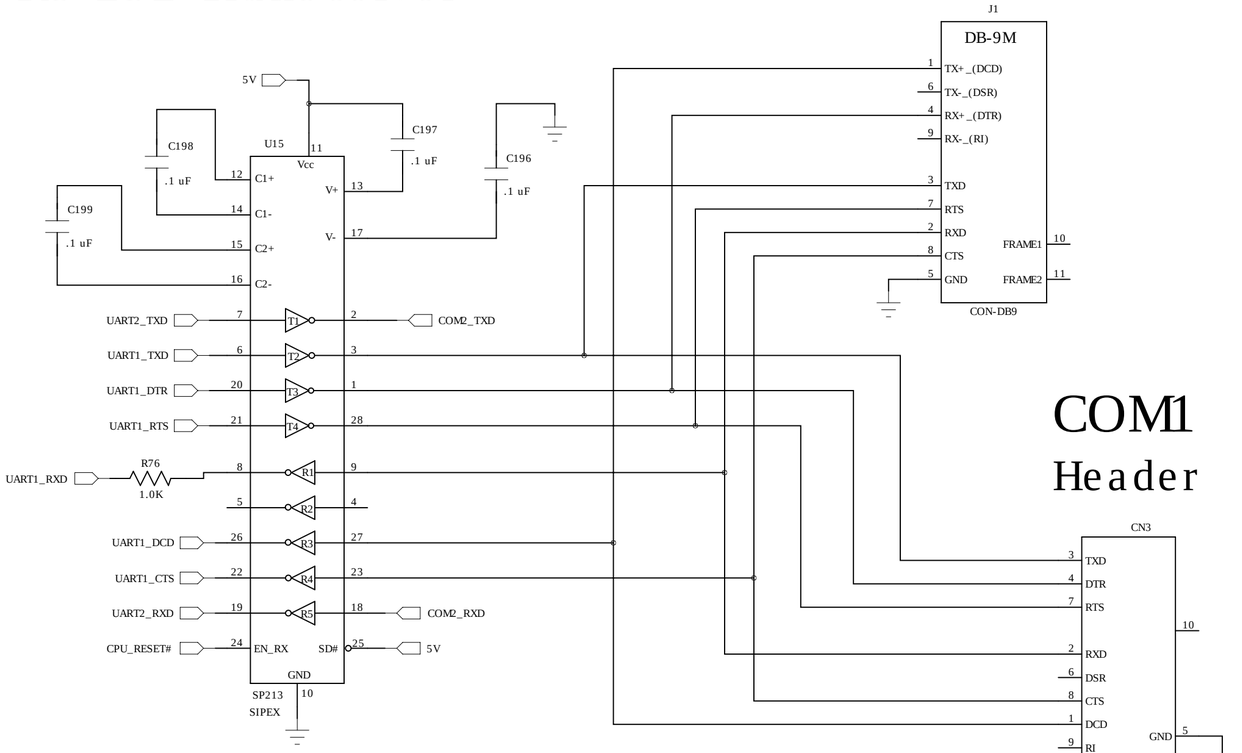
Right LED (Amber)
100 Mbit

Left LED (Green)
Link / Activity

Technologic Systems	Date March 15, 2008	
Title: TS-7350 Power Supplies, Ethernet		
Rev:	Designer RLM	Sheet 3 of 7

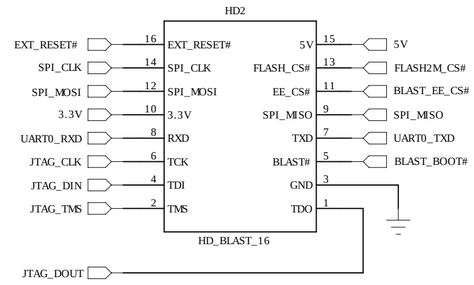
COM1
DB9M

RS-232 Transceiver

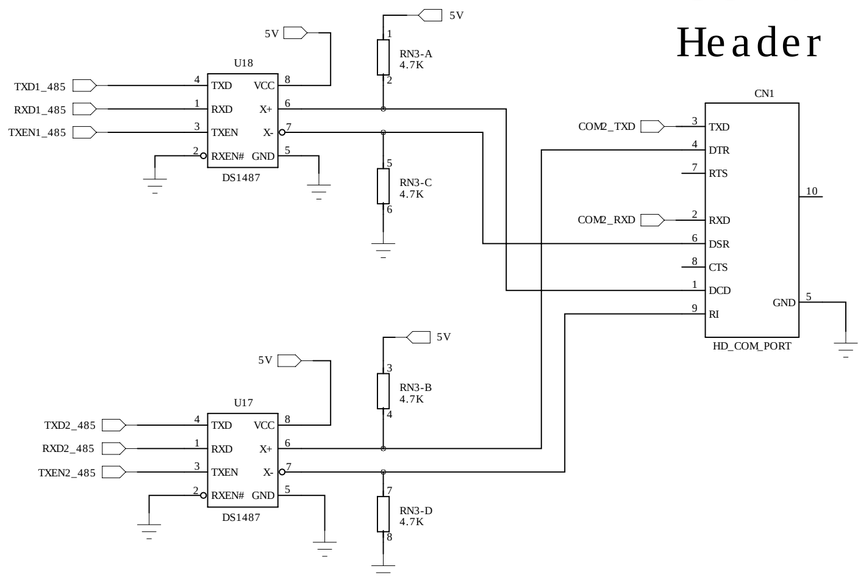


COM1
Header

JTAG
16-pin
Header



RS-485 Drivers



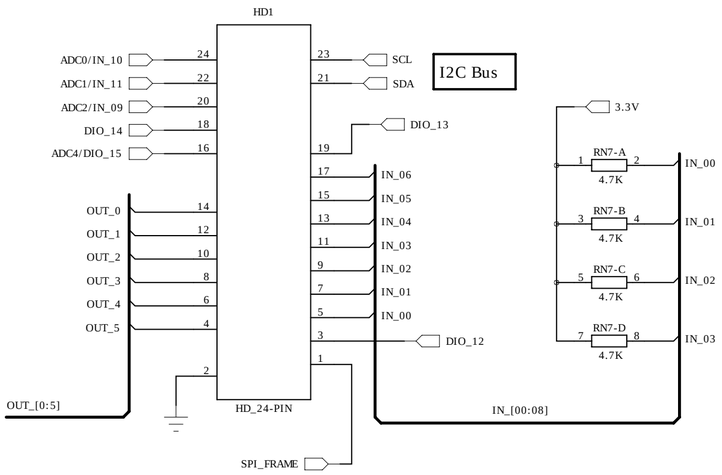
COM2
Header

UART0 and UART1 are in the EP9302 CPU chip

UART2 thru UART9 are X-UARTs in the FPGA

UART0 drives TTL levels to the JTAG header (TXD and RXD only)
UART1 drives COM1 TXD and RXD (RTS, CTS, DTR, DCD are from FPGA)
UART2 drives COM2 (TXD and RXD only)
UART3 and UART4 drive RS-485 ports
UART5 and UART6 drive COM1 handshakes
UART7 and UART8 drive PC/104 bus (TTL levels)
UART9 drives DIO header (TTL levels)

DIO Header



24-pin Header

24 + 16 = 40-pin Header

4 ADC
ADC lines in parallel with
IN_09, IN_10, IN11, DIO15

2 I2C
1 GND
6 Latched Outputs (OUT0-OUT5)
7 Buffered Inputs (IN0-IN6)
3 DIO_12, DIO_13, DIO_14
1 SPI_FRAME

Technologic Systems	Date March 15, 2008	
Title: TS-7350 COM Ports DIO JTAG Headers		
Rev:	Designer	Sheet 4 of 7

Lattice XP2 FPGA

XP2-5 has:
5K LUTS 2 PLLs
9 blocks of 1Kx18 Block RAM
12 18x18 Multipliers
146 I/O with 208 pin package
"instant ON" = about 1.5 mS
input PLL clock = 10 MHz min

Make sure these signals are on CLK inputs:
SDRAM_CLK
FPGA_25MHz

PROGRAM#, DONE, and INIT# are dedicated configuration pins when CFG0 is low. When CFG0 is high they are "general purpose I/O"
Page 4 of TN1141

During JTAG Flash programming the PROGRAM# pin should be high else it can inhibit Flash --> SRAM
DONE likewise must be high
These do have weak PU resistors

When CFG0 = 1 then always uses SDM
SDM = Self Download Mode
SDM uses on-chip Flash --> SRAM
CFG0 PU resistor uses VCC core (1.2V)

TAG Memory is 79 bytes of Flash (XP2-5)
Always available thru JTAG port
can not be Write or Read protected
perfect for: MAC, birth date, Revision #
TAG memory can be accessed from fabric

Set CONFIG_MODE to NONE
This allows all pins to be used

ADD[00:24]
DATA_[00:15]
ISA_ADD[00:19]
ISA_D[00:15]
AUX_D[0:7]
SD_ADD[00:11]
SD_DATA_[00:15]

ADD00 148 IO
ADD01 156 IO
ADD02 173 IO
ADD03 169 IO
ADD04 186 IO
ADD05 180 IO_CLK
ADD06 185 IO_CLK
ADD07 187 IO
ADD08 175 IO
ADD09 168 IO
ADD10 142 IO
ADD11 164 IO_PLL_TIN
ADD12 183 IO_CLK
ADD13 136 IO
ADD14 155 IO
ADD15 163 IO_PLL_CIN
ADD16 125 IO_CLK
ADD17 121 IO
ADD18 124 IO
ADD19 9 IN_CFG1
ADD20 123 IO_CLK
DQM1# 134 IO_CLK
CS6# 8 IN_PROGRAM#
EP_RD# 120 IO
EP_WR# 137 IO
FGPA_25MHZ 105 IO
JTAG_CLK 114 IO
111 IO
TSLOCK_DATA 28 TOE
115 IP
35 IO
ISA_ADD09 32 IO_CLK
ISA_ADD08
ISA_ADD07 36 IO
ISA_ADD06 40 IO
ISA_ADD05 43 IO
ISA_ADD04 45 IO
ISA_ADD03 34 IO
ISA_ADD02 42 IO
ISA_ADD01 52 IO
ISA_ADD00 46 IO
ISA_ADD11
ISA_ADD10 21 IO_INIT#
22 IO_CLK
ETH2_CS# 116 IO
29 CFG0 (PU resistor)
JTAG_DOUT 129 JTAG_DOUT
JTAG_DIN 128 JTAG_DIN
JTAG_CLK 127 JTAG_CLK
JTAG_TMS 126 JTAG_TMS

IO 159 DATA_00
IO_PLL_TFB 160 DATA_01
IO 170 DATA_02
IO_PLL_CFB 158 DATA_03
IO 157 DATA_04
IO 150 DATA_05
IO 151 DATA_06
IO 174 DATA_07
IO 193 DATA_08
IO 167 DATA_09
IO 176 DATA_10
IO 177 DATA_11
IO 184 DATA_12
IO 178 DATA_13
IO_CLK 179 DATA_14
IO 189 DATA_15
IO 2 ISA_B06
IO 122 ISA_B08
IO_CLK 23 ISA_B15
IO 6 ISA_B16
IO 18 ISA_ADD13
IO 31 ISA_IOCHK
IN_CSSPIS 11 ISA_READY
IO 51 ISA_OSC
IO_CCLK 17 ISA_MEMR#
IO 12 ISA_MEMW#
OUT_CSSPIN 13 ISA_IOR#
IO 1 ISA_IOW#

IO 33 ISA_D15
IO 47 ISA_D14
IO 44 ISA_D13
IO 19 ISA_D12
IO 41 ISA_D11
IO_CLK 135 ISA_D10
IO 7 ISA_D09
IO 207 ISA_D08
IO 195 ISA_D07
IO 197 ISA_D06
IO 188 ISA_D05
IO 198 ISA_D04
IO_PLL_CIN 206 ISA_D03
IO_PLL_CFB 201 ISA_D02
IO_PLL_TIN 208 ISA_D01
IO_PLL_TFB 202 ISA_D00

U16
LATTICE_XP2_208

3.3V 200 VCCO_0
191 VCCO_0
172 VCCO_1
166 VCCO_1
152 VCCO_2
141 VCCO_2
117 VCCO_3
107 VCCO_3
95 VCCO_4
89 VCCO_4
70 VCCO_5
61 VCCO_5
50 VCCO_6
38 VCCO_6
5 VCCO_7
16 VCCO_7
25 VCC_AUX1
80 VCC_AUX2
132 VCC_AUX3
181 VCC_AUX4
130 VCC_JTAG
57 VCC_PLL_0
99 VCC_PLL_1
162 VCC_PLL_2
204 VCC_PLL_3
1.2V 4 VCC_INT1
26 VCC_INT2
27 VCC_INT3
49 VCC_INT4
79 VCC_INT5
108 VCC_INT6
131 VCC_INT7
153 VCC_INT8
182 VCC_INT9

AUX_D0 196 IO
AUX_D1 146 IO
AUX_D2 147 IO
AUX_D3 149 IO
AUX_D4 138 IO
AUX_D5 139 IO
AUX_D6 145 IO
AUX_D7 140 IO

IO 93 SD_ADD00
IO_PLL_TIN 97 SD_ADD01
IO_PLL_CIN 98 SD_ADD02
IO_PLL_TFB 101 SD_ADD03
IO 85 SD_ADD04
IO_CLK 81 SD_ADD05
IO_CLK 78 SD_ADD06
IO 75 SD_ADD07
IO 74 SD_ADD08
IO 73 SD_ADD09
IO 94 SD_ADD10
IO 72 SD_ADD11
IO 88 SD_BA0
IO 91 SD_BA1
IO 87 SD_RAS#
IO 86 SD_CAS#
IO 84 SD_WE#
IO_CLK 76 SDRAM_CLK

IO 64 SD_DATA_00
IO 65 SD_DATA_01
IO 66 SD_DATA_02
IO 67 SD_DATA_03
IO 68 SD_DATA_04
IO 77 SD_DATA_05
IO_CLK 82 SD_DATA_06
IO 83 SD_DATA_07
IO 63 SD_DATA_08
IO_PLL_CFB 60 SD_DATA_09
IO_PLL_TFB 59 SD_DATA_10
IO_PLL_CIN 55 SD_DATA_11
IO 54 SD_DATA_12
IO 56 SD_DATA_13
IO_PLL_TIN 53 SD_DATA_14
IO 69 SD_DATA_15
IO_PLL_CFB 103 SDCARD_CLK
IO 104 SDCARD_COM
IO 102 SDCARD_D0
IO 92 SDCARD_D1
IO 112 SDCARD_D2
IO 110 SDCARD_D3
IO 106 RD_BUF1#
IO 144 RD_BUF2#
IO 118 WR_LATCH1
IO 205 WR_LATCH2
IO 20 WR_LATCH3
IO_DONE 10 ISA_ADD12
IO_CLK 30 ISA_AEN
IO 15 ISA_REFRESH#
IO 194 RTC_ALE
IO 192 RTC_CS#
IO 39 WAIT#
IO 113 DMA_REQ

GND1 3
GND2 14
GND3 24
GND4 37
GND5 48
GND6 58
GND7 62
GND8 71
GND9 90
GND10 96
GND11 100
GND12 109
GND13 119
GND14 133
GND15 143
GND16 154
GND17 161
GND18 165
GND19 171
GND20 190
GND21 199
GND22 203

Pull-up and pull-down resistors are 6 to 30K ohms

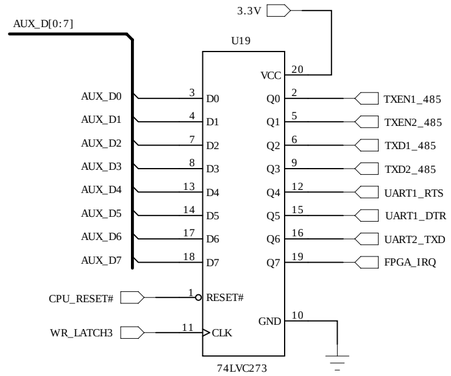
8 MB Video SDRAM

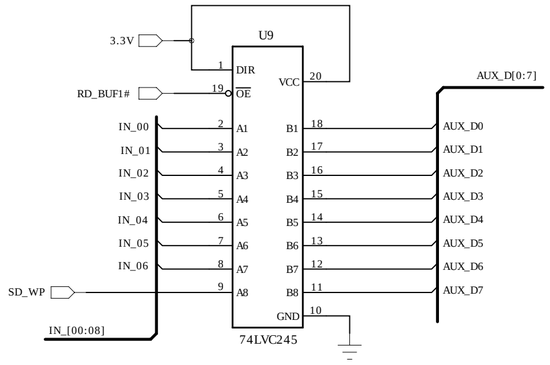
U14
3.3V
SD_ADD00 23 A0
SD_ADD01 24 A1
SD_ADD02 25 A2
SD_ADD03 26 A3
SD_ADD04 29 A4
SD_ADD05 30 A5
SD_ADD06 31 A6
SD_ADD07 32 A7
SD_ADD08 33 A8
SD_ADD09 34 A9
SD_ADD10 22 A10
SD_ADD11 35 A11
36 A12
SD_BA0 20 BA0
SD_BA1 21 BA1
SD_RAS# 18 RAS#
SD_CAS# 17 CAS#
SD_WE# 16 WE#
3.3V 37 CKE
SDRAM_CLK 38 CLK
15 DQML
39 DQMH
19 CS#
VCCINT 1
VCCINT 14
VCCINT 27
VCCIO 3
VCCIO 9
VCCIO 43
VCCIO 49
DQ0 2 SD_DATA_00
DQ1 4 SD_DATA_01
DQ2 5 SD_DATA_02
DQ3 7 SD_DATA_03
DQ4 8 SD_DATA_04
DQ5 10 SD_DATA_05
DQ6 11 SD_DATA_06
DQ7 13 SD_DATA_07
DQ8 42 SD_DATA_08
DQ9 44 SD_DATA_09
DQ10 45 SD_DATA_10
DQ11 47 SD_DATA_11
DQ12 48 SD_DATA_12
DQ13 50 SD_DATA_13
DQ14 51 SD_DATA_14
DQ15 53 SD_DATA_15
GND 6
GND 12
GND 46
GND 52
GND 28
GND 41
GND 54
SDRAM16
DNP

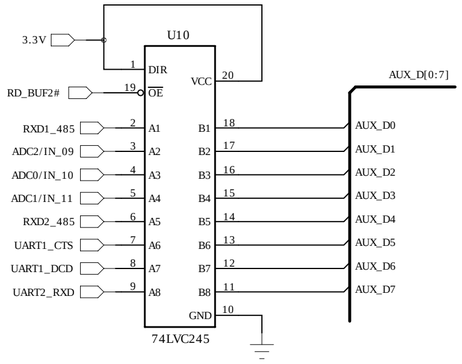
CPU_RESET is the same as PWR_RST# (as in TS-7xxx)
In previous products, it was the OR of LOW_VOLT# and the WatchDog time-out

Page 37 of Data Sheet (Hot Socketing)
Power Supplies can be sequenced in any order but must be monotonic
All I/O lines are tri-stated during power cycling

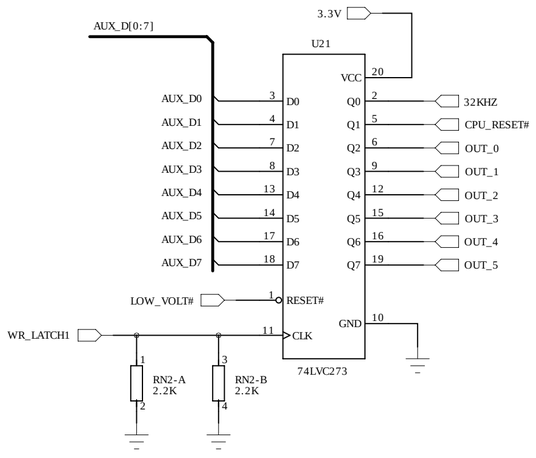
Technologic Systems	Date March 15, 2008	
Title: TS-7350 FPGA and Frame Buffer		
Rev:	Designer	Sheet 5 of 7

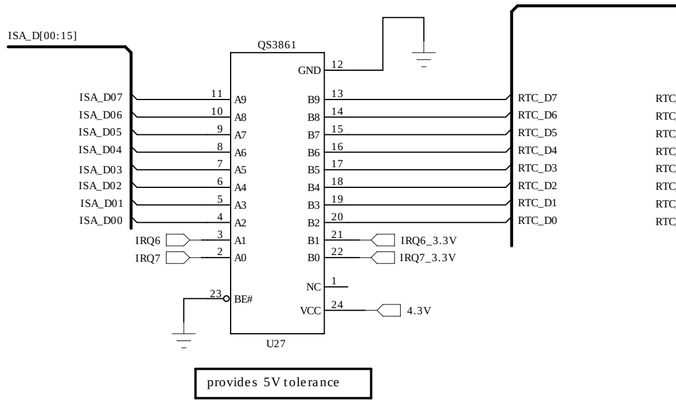




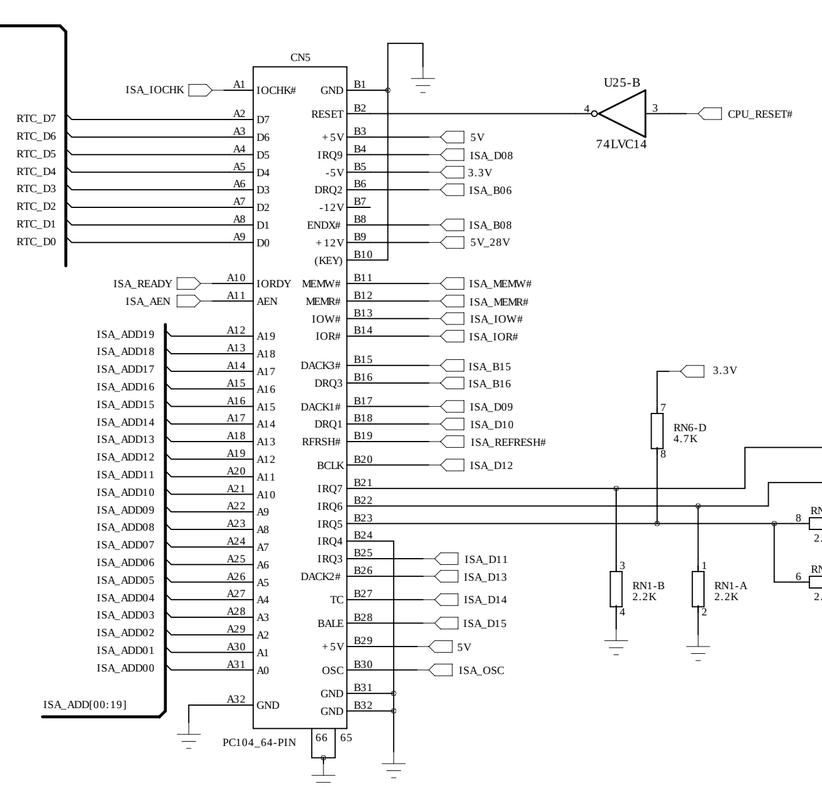


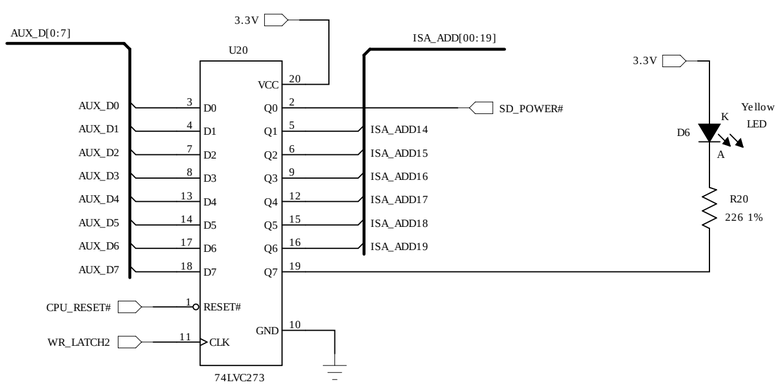
PC/104 64-pin Connector

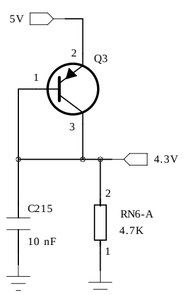




provides 5V tolerance







Warning:

All IRQs and data lines D0-D7 are 5V tolerant

all other signals must use 3.3V levels

IRQ3 must be 3.3V levels

33 lines directly into FPGA

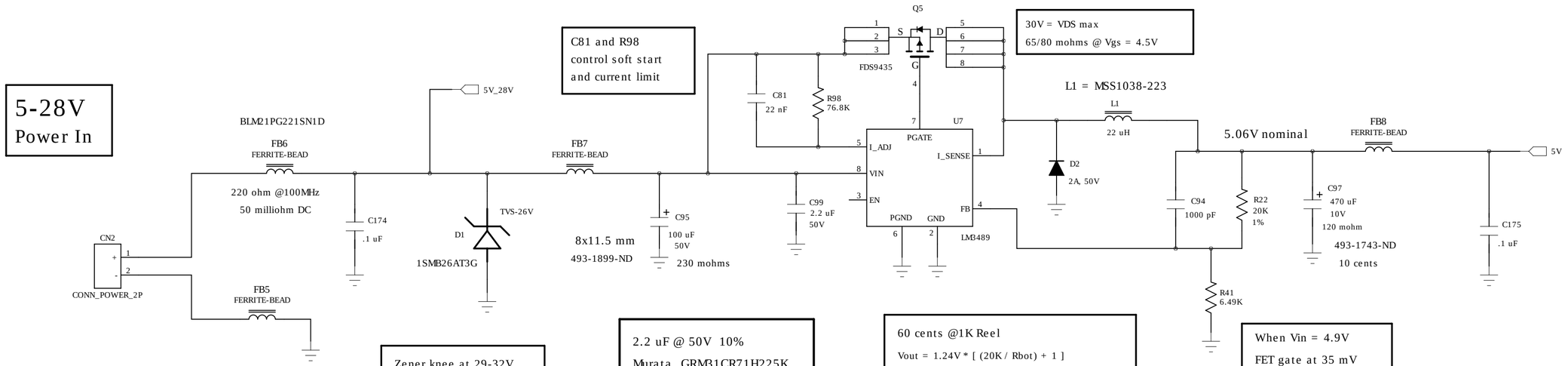
plus 10 more (D0-D7 and IOR, IOW) that can be used with no RTC option

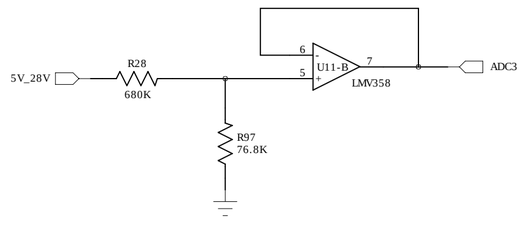
plus 6 more from latch (A14-A19)

Technologic Systems	Date March 15, 2008	
Title: TS-7350 PC/104 AUX Bus		
Rev:	Designer	Sheet 6 of 7

Hysteretic Switching Power Supply

5V @ (2.5 Amps)





Technologic Systems	Date March 15, 2008	
Title: TS-7350 5V Power Supply		
Rev:	Designer	Sheet 7 of 7