March 6, 2006

Ms. Sandra Mandawe
LGC Wireless, Inc.
2540 Junction Avenue
San Jose, CA 95134

Dear Ms. Mandawe,

Attached is the Highly Accelerated Life Test Report for the Technologic Systems TS-7250. Testing was conducted from February 21st through 23rd, 2006, at QualMark Labs in Santa Clara.

In the HALT testing the product performed quite well, but there are some areas that need investigation and corrective action:

a) Flash data corruption in the Cold Step Stress Test.
b) Failure to communicate with the test bench in the Hot Step Stress Test.
c) Intermittent power connection in the Vibration Step Stress Test.
d) Intermittent USB connection in the Vibration Step Stress Test.
e) Dim Green LED in the Combined Environment Test.

Benefits available from other Reliability Tools:

- Early Knowledge of Problem Components with **MTBF Parts Stress Predictions**
- Early Knowledge of Wearout Issues with **End-of-Life Predictions**
- Establish Risks with **FMECA** (Failure Modes Effects and Criticality Analysis)
- Measure your product's MTBF with **Reliability Demonstration Tests**
- Multiply value with **Reliability Integration** by using individual reliability tools in conjunction with all of the other tools

Please contact us for more details on these services. We look forward to being of further assistance in your overall product reliability program.

Sincerely,

Mike Silverman, C.R.E.
Managing Partner, Ops A La Carte LLC

HIGHLY ACCELERATED LIFE TEST REPORT #1358

Technologic Systems Single Board Computer – TS-7250

Prepared for:

Ms. Sandra Mandawe
LGC Wireless, Inc.
2540 Junction Avenue
San Jose, CA 95134

Highly Accelerated Life Test Report

Test Dates: 2/21/06 – 2/23/06

Single Board Computer – TS-7250

Testing Performed for:
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Test Report Reviewed by:
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Mike Silverman, CRE

Reference Documents			
Document	**Revision**	**Number**	**Date Issued**
HALT Test Plan	N/A	#1358	02/21/06

1. Objective

Highly Accelerated Life Testing (HALT) is performed to uncover latent defects in product design, component selection and/or manufacturing that would not otherwise be found through conventional qualification methods. The process subjects the test product to progressively higher stress levels, incorporating thermal dwells, rapid temperature transitions, vibration, and a combination of temperature and vibration to precipitate inherent defects. Moreover, HALT stresses the product to failure in order to assess design robustness and margin above its intended operation.

2. Scope

To find the weak links in product design, document failure modes, and determine the true operating and destruct limits using repeatable testing techniques such as thermal step stress, rapid thermal transitions, vibration step stress, and combined temperature and vibration environments. By subjecting the product to increasing levels of stress, long term failure modes that would show up under normal operating conditions in months or years can be revealed in just hours or days.

An essential component of HALT is root cause analysis and the identification and implementation of corrective action to ensure the product integrity, thus increasing the product's reliability and the robustness of design.

3. Acronyms and Definitions

- HALT – Highly accelerated life test
- UUT – Unit under test
- Operating Limit (OL) - The operating limit is defined as the last operational temperature or vibration set point prior to failure.
- Destruct Limit (DL) - The destruct limit is the level at which the product stops functioning and remains inoperable at normal operating conditions.
- Grms – Gravity Root Means Squared

4. Test Summary

Table 1: Operating and Destruct Limits

Stress Condition	Chamber Setpoint
Cold Temperature OL	-50°C
Hot Temperature OL	+110°C
Vibration OL	25 Grms
Cold Temperature DL	-60°C
Hot Temperature DL	>+120°C
Vibration DL	> 55 Grms

Highlights of failure modes and weaknesses discovered during the HALT process:

Thermal Step Stress:

- Cold Step Stress - At -60°C corrupted data appeared in the flash memory of 3 of the 4 test items.
- Hot Step Stress - At +120°C, both serial and Ethernet communications were lost with all four UUTs. It was noticed at that time that UUTA was automatically rebooting. The other UUTs may have also been rebooting, but it was not noticed.

Rapid Thermal Transitions:

- There were no problems noted during this test.

Vibration Step Stress:

- At 10 Grms and 20 Grms, there were some cases in which the UUTs would reboot by themselves. This may have been due to the vibration affecting the power supply connector at the PCB. (Combined Environment Testing on Day 3 used a soldered power connection to the UUT in lieu of the power connector. See results in paragraph 9.6.)
- At 30 Grms and higher, failures were seen related to USB communication.
- At 40 Grms and higher, UUTs started rebooting by themselves. Also saw one instance of the Ethernet test failing.

Combined Environment:

- Initially, at low vibration levels the UUTs had intermittent power connections at the PCB/PS connector interface. The connectors were removed and the PS wires were soldered directly to the PCB pins. This resolved that problem.
- During the first two cycles, the upper temperature limit was +110°C, but at that level there were numerous problems attempting to communicate with the UUTs. When the temperature was dropped back to +100°C, communication was reestablished.
- At the cold portion of the temperature cycle with vibration, problems with the USB Test were seen. The USB connector cannot handle vibration – this is an industry known problem.

- On the 11th cycle at -85°C and 65 Grms (very extreme levels), the test diagnostics could not communicate with UUTC. Upon return to ambient, UUTC began to work, but the Green LED on the PCB was very weak. As the PCB warmed up, the LED returned to normal, and UUTC then passed all tests.

5. Typical Failures by Stress:

Below is a summary of typical failures found in each stress applied during HALT. These tables are excerpts from Mike Silverman's paper entitled, "HALT and HASS Summary at an Accelerated Reliability Test Center."

Table 2a – TYPICAL FAILURES DURING COLD STEP STRESS

Failure Mode
Circuit design issue
Intermittent component

TABLE 2b – TYPICAL FAILURES DURING HOT STEP STRESS

Failure Mode
Failed component
Circuit design issue
Degraded component

TABLE 2c – TYPICAL FAILURES DURING RAPID TEMPERATURE TRANSITIONS

Failure Mode
Cracked component
Intermittent component
Failed component
Cold or insufficient solder

TABLE 2d – TYPICAL FAILURES DURING VIBRATION STEP STRESS

Failure Mode
Broken lead
Screws back out
Socket failures
Connector backs out
Tolerance issue
Card backs out
Shorted component
Broken component
RTV applied incorrectly
Potentiometer turns
Plastic cracks at stress point
Intermittent component
Failed component
Connectors wearing
Connector making intermittent contact
Connector breaks from board
Broken trace

TABLE 2e – TYPICAL FAILURES DURING COMBINED ENVIRONMENT

Failure Mode
Broken lead
Component falls off (non-soldered)
Failed component
Broken component
Component shorted out
Cracked potting material
Detached wire
Circuit design issue
Socket failures

6. Products Tested

The units subjected to the HALT process are documented below. Each board is a TS-7250 production board, Rev. A.

Table 3: Product Identification

Description	MAC Address	Serial number
Board A	00:D0:69:40:2E:84	0040832
Board B	00:D0:69:40:2E:86	0040831
Board C	00:D0:69:40:2E:7E	0040823
Board D	00:D0:69:40:2E:87	0040235

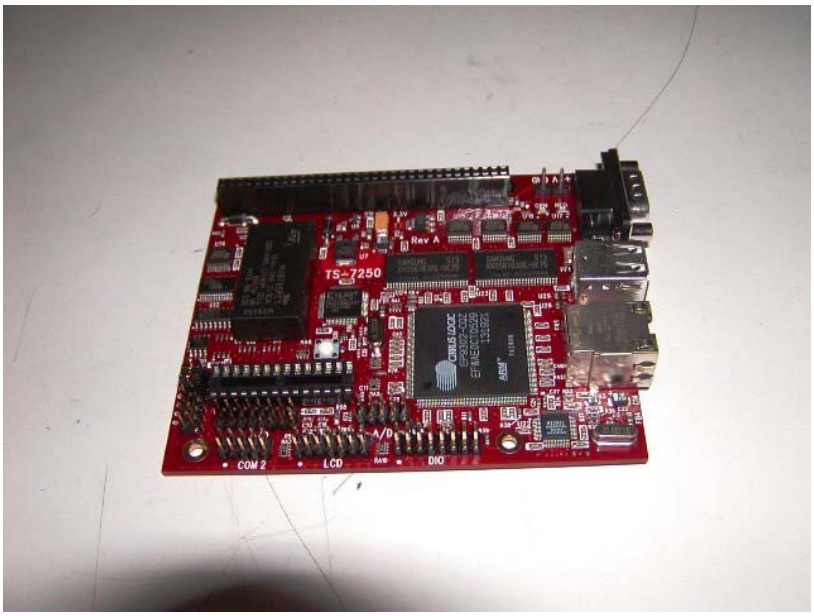


Figure 1: Technologic Systems TS-7250 Single Board Computer

7. Test Equipment and Setup

7.1 Test Equipment

Equipment used to conduct the HALT testing is detailed below. Any test equipment that required periodic calibration was in current calibration at time of test. The calibration certifications are traceable to the National Institute of Standards and Technology.

Table 4: Customer Test Equipment

Description	Manufacturer	Model number
8 Port Hub	Linksys	EWHUB
RS232 4 Port Switch Box	Unknown	N/A
Notebook Computer	Sony	VAIO
Loop Back Boards – COM & DIO	TS	N/A

Table 5: Lab Test Equipment

Description	Manufacturer	Model number	Serial Number	Calibration Due
HALT Chamber	QualMark	Typhoon 2.5	134	See Below
Data Logger	Fluke	Hydra 2620A	6516303	3/10/06
Thermocouples	Omega	C03-T-60 / TT-T-30		NA
Accelerometer Ch. 5	Dytran	3032M1	147/10.7	2/24/06
Accelerometer Ch. 2	Dytran	3032M1	196/9.8	2/24/06
Accelerometer Ch. 3	PCB	VA320B13/005L	994/4.87	5/27/06
Accelerometer Ch. 4	Dytran	3030A4	4808/10.4	6/27/06
Accelerometer Control	Dytran	3030B5U	4889/10.3	6/27/06
Spectrum Analyzer	QualMark	Model 2.0		N/A
Data Acquisition Card	National Instru.	PCI-6023E	0x11551F2	6/26/06
Signal Conditioner	PCB	482A05	1519	10/13/06

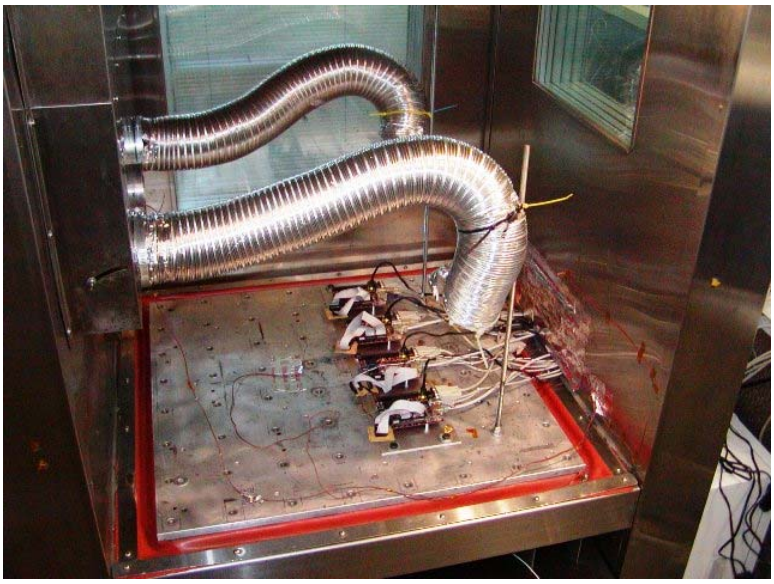


Figure 2: HALT Chamber and Test Item Setup

7.2 Temperature Test Setup

During the thermal testing airflow from the chamber was directed onto the UUTs using 4" aluminum ducting. This allowed for better temperature stabilization during the thermal step stress and faster ramp rates during the rapid thermal transition process. The UUTs were mounted with ½ inch standoffs to a ½ inch plate which was bolted to the vibration table. Thermocouples were attached to the UUTs to monitor the temperature of the product at various locations. Two of the boards had voltage monitoring wires connected to monitor the 3.3VDC. The locations of the thermocouple placements and voltage monitoring wires are located in the table below. Pictures illustrating the temperature test setup are located in Appendix A.

Table 6: Data collection points for temperature and voltage monitoring.

Fluke Data logger Channel Assignment		
Channel	**Type**	**Location or Description**
1	TC	UUT #A – Cirrus Logic EP9302(CPU) IC
2	TC	UUT #A – Altera MAX II(CPLD) IC
3	TC	UUT #B – Cirrus Logic EP9302(CPU) IC
9	TC	UUT #B – Altera MAX II(CPLD) IC
5	TC	UUT #C – Cirrus Logic EP9302(CPU) IC
6	TC	UUT #C – Altera MAX II(CPLD) IC
7	TC	UUT #D – Cirrus Logic EP9302(CPU) IC
8	TC	UUT #D – Altera MAX II(CPLD) IC
12	Voltage	UUT #A – 3.3 VDC
13	Voltage	UUT #B – 3.3 VDC

7.3 Vibration Test Setup

The four UUTs were mounted to a ¼ inch thick plate with ½ inch standoffs. The plate was bolted to the vibration table at six locations using 3/8" – 16 bolts. Pictures illustrating the fixture setup are located in Appendix A.

Accelerometers were attached to the UUT to measure the vibration response on the product at various locations. The location of each accelerometer is located in the table below. More detailed pictures illustrating the vibration fixture and the locations of accelerometers are located in Figure 2 and Appendix A.

Table 7: Accelerometer Locations.

Spectrum Analyzer Channel Assignment		
Channel	**Axis**	**Location or Description**
5	Z	Mounted on UUT#A
2	Z	Mounted on UUT#B
3	Z	Mounted on UUT#D
4	Z	Mounted underneath the vibration table at center.

Note: The X-axis runs through the chamber doors, the Y-axis runs from the access portal to air plenum, and the Z-axis is vertical to the vibration table.

8. Functional Test Description

The functional test consisted of the following tests and were conducted on each of the UUTs:

1. Power Cycle – Before the set of tests listed below, the UUTs were power cycled.
2. DIO Test - A test harness was used to short 10 DIO/LCD pins with the other 10 DIO/LCD pins.

   Loop back pin out

   DIO_0 -> LCD_0
   DIO_1 -> LCD_1
   DIO_2 -> LCD_2
   DIO_3 -> LCD_3
   DIO_4 -> LCD_4
   DIO_5 -> LCD_5
   DIO_6 -> LCD_6
   DIO_7 -> LCD_7
   DIO_8 -> LCD_WR
   LCD_EN -> LCD_RS

   A. Configured the first set as outputs and the second set as inputs.

B. Asserted each output pin and checked to ensure the corresponding input pin was also asserted.
C. De-asserted each output pin and checked to ensure that the corresponding input pin was also de-asserted.
D. Configured the outputs as inputs and the inputs as outputs and repeated the process.

3. Com Test - A test harness was used to short the handshake lines, and Tx to Rx.

   Loop back pin out

   DTR -> DSR
   DTR -> DCD
   RTS -> CTS
   RX -> TX

   A. Asserted DTR and ensured DSR and DCD were also asserted.
   B. Asserted RTS and verified CTS was asserted.
   C. De-asserted DTR and checked DSR and DCD to ensure they were de-asserted.
   D. De-asserted RTS and then checked CTS to ensure it was de-asserted.
   E. Sent out two bytes (0x55 and 0xAA) and ensured they were received.

4. USB Test - A USB flash drive was plugged into each USB port.
   A. Under software control, power cycled the USB port to simulate hot plugging the USB devices.
   B. Queried each USB device for its cylinders, heads, and sectors. Verified that these were non-zero values.

5. Ethernet Test - The board was pinged 10 times.
6. Flash Memory Test – The flash memory was tested to verify no bad blocks.

When a failure occurred, the test diagnostics logged the failure data, and attempts to determine the cause of failure were made.

Test equipment used to monitor the UUTs was set up on a bench outside the HALT chamber. Cables, wires, and power cords were fed through the chamber access port.

8.1 Failure Characterization

During the HALT process, any abnormalities were considered possible failure modes until they could be determined otherwise. To establish clear failure characterization the list below details acceptable specifications and/or unit functionality.

The acceptance criteria for the above tests were –

1. Power Cycle - UUTs must turn off and back on under all test conditions.

2. DIO Test - A failure will occur when an output pin is not in the same state as the corresponding input pin. There must also be continuity between the output pin and the input pin.

3. COM Test - A failure will occur when an output pin is not in the same state as the corresponding input pin. There must also be continuity between the output pin and the input pin. A failure will also occur if the two bytes that were sent are not received back.

4. USB Test - A failure will occur when we are unable to query either of the USB flash drives for its cylinders, heads, or sectors.

5. Ethernet Test - A failure will occur when all 10 pings fail.

6. Flash Memory Test – A failure will occur if any bad blocks are detected.

8.2 Fault Recovery

When a failure occurred, the environmental stress was reduced to determine when the UUT recovered. Once the UUT recovered, the environmental stress was increased to determine if the failure mode was repeatable.

1. If the UUT was still functional after repeating the failure mode, the environmental stress was increased until additional failure modes were determined or a hard failure occurred.
2. If the UUT was not functional after repeating the failure mode, an attempt was made to mask the failure and continue testing in pursuant of additional failure modes.

9. HALT Results

9.1 Cold Temperature Step Stress

The cold temperature step stress began at +20°C and decreased in 10°C increments. The dwell time at each thermal step was 10 minutes. The dwell time began after the component temperatures on the UUTs stabilized. Airflow from the chamber was directed onto the UUTs using 4" aluminum ducting, and the UUTs were placed on standoffs to prevent the boards from heat sinking to the vibration table. The UUTs were monitored for functionality throughout the cold temperature step stress process.

The following abnormalities were noted during the test –

1. At -60°C corrupted data appeared in the flash memory of UUTB, UUTC, and UUTD. The temperature was raised to -55°C, but the problem remained. This is a failure mode that will not recover; once the data is corrupted, it has to be reloaded.
2. Back at ambient conditions the data was reloaded into the flash memory on each of the three failed boards.

Lower Operating Limit (LOL): -50°C

Lower Destruct Limit: (LDL): -60°C

Table 8: Cold Step Stress Results

Chamber Set point (°C)	Pass/Fail	Comments
+10	Pass	Power Cycle – ABCD; DIO – ABCD; COM - ABCD; USB – ABCD Ethernet – ABCD; Flash - ABCD
0	Pass	Power Cycle – ABCD; DIO – ABCD; COM - ABCD; USB – ABCD Ethernet – ABCD; Flash - ABCD
-10	Pass	Power Cycle – ABCD; DIO – ABCD; COM - ABCD; USB – ABCD Ethernet – ABCD; Flash - ABCD
-20	Pass	Power Cycle – ABCD; DIO – ABCD; COM - ABCD; USB – ABCD Ethernet – ABCD; Flash - ABCD
-30	Pass	Power Cycle – ABCD; DIO – ABCD; COM - ABCD; USB – ABCD Ethernet – ABCD; Flash - ABCD
-40	Pass	Power Cycle – ABCD; DIO – ABCD; COM - ABCD; USB – ABCD Ethernet – ABCD; Flash - ABCD
-50	Pass	Power Cycle – ABCD; DIO – ABCD; COM - ABCD; USB – ABCD Ethernet – ABCD; Flash - ABCD
-60	Fail	Power Cycle – ABCD; DIO – ABCD COM - ABCD; USB – ABCD Ethernet – ABCD Flash – A passed; B- flash failures; C-flash failures; D-flash failures;
-55	Fail	Power Cycle – ABCD; DIO – ABCD COM - ABCD; USB – ABCD Ethernet – ABCD Flash – A passed, B- flash failures; C-flash failures; D-flash failures;

Table 9: Temperatures and Voltages Recorded During the Cold Temperature Step Stress

Set point (°C)	UUTA U8	UUTA U19	UUTB U8	UUTB U19	UUTC U8	UUTC U19	UUTD U8	UUTD U19	UUTA VDC12	UUTB VDC13
+20	27.9	27.2	29.3	27.5	28.0	28.5	27.5	27.4	3.302	3.322
+10	14.7	14.1	16.5	14.3	14.4	15.1	14.1	14.3	3.303	3.323
0	4.7	3.9	6.5	4.3	4.3	5.0	4.0	4.3	3.303	3.323
-10	-4.9	-5.5	-3.1	-5.1	-5.2	-4.7	-5.7	-5.3	3.303	3.323
-20	-15.1	-15.6	-12.7	-15.2	-15.5	-14.6	-15.7		3.303	3.323
-30	-25.6	-26.0	-23.0	-25.5	-25.9	-25.2	-26.2		3.303	3.322
-40	-36.0	-36.9	-33.3	-36.2	-36.2	-36.4	-37.1		3.301	3.321
-50	-46.0	-46.9	-43.4	-46.2	-46.1	-46.4	-47.0		3.300	3.319
-60	-55.7	-57.0	-53.2	-55.8	-55.9	-56.4	-57.0		3.298	3.317

Note: Thermocouple Locations are documented in Table 6.

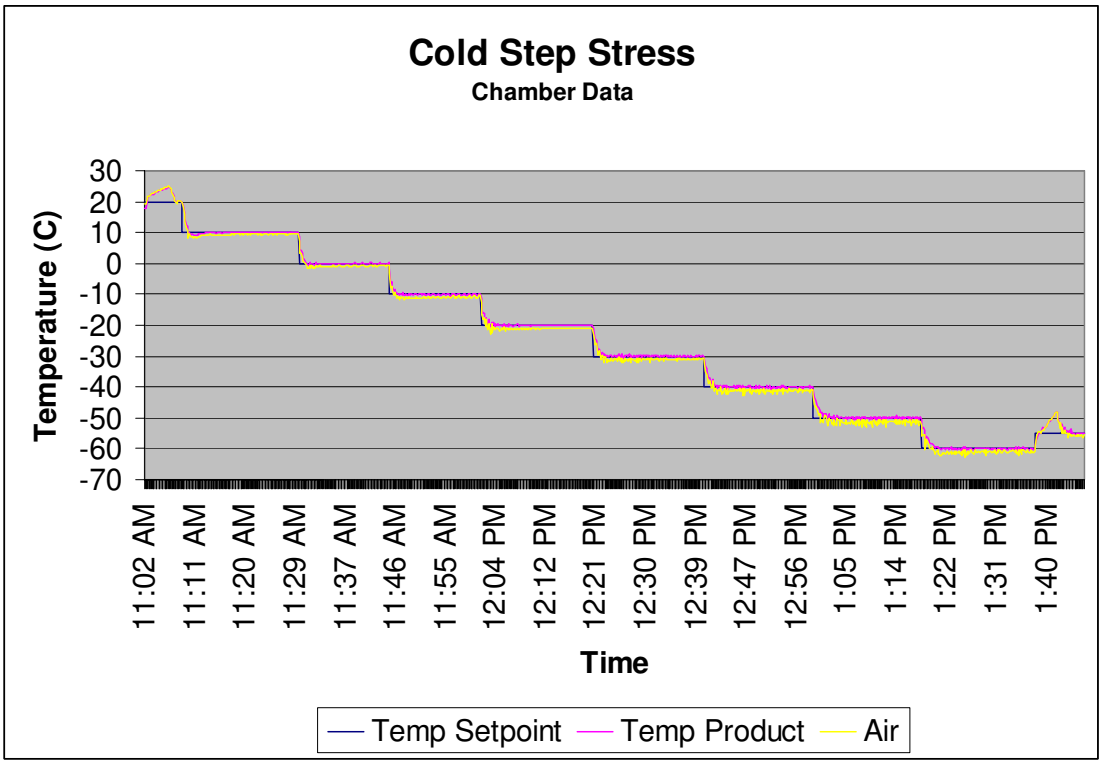


Figure 3: Cold Step Stress Test – Chamber Data

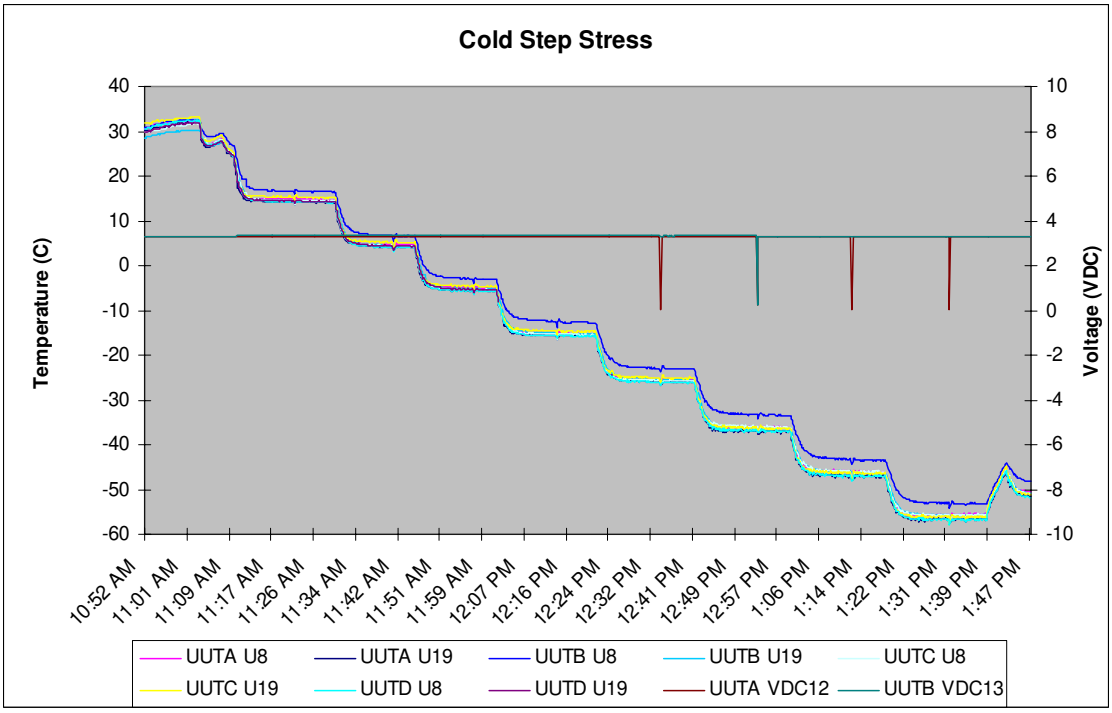


Figure 4: Cold Step Stress Test – Thermocouple and Voltage Readings

9.2 Hot Temperature Step Stress

The Hot temperature step stress began at +30°C and increased in 10°C increments. The dwell time at each thermal step was 10 minutes. The dwell time began after the component temperatures on the UUTs stabilized. Airflow from the chamber was directed onto the UUT using 4" aluminum ducting, and the UUTs were placed on standoffs to prevent the boards from heat sinking to the vibration table. The UUTs were monitored for functionality throughout the hot temperature step stress process.

The following abnormalities were noted during the test –

1. At +120°C, both serial and Ethernet communications were lost with all four UUTs. It was noticed at that time that UUTA was automatically rebooting. The other UUTs may have also been rebooting, but it was not noticed. The data logger for UUTB 3.3 VDC shows that is dropped to 0 Volts several times during this period.
2. At +115°C, after recycling the input power, UUTA passed all tests, and at +110°C UUTC and UUTD recovered. UUTB did not recover until the chamber was rapidly dropped from +110°C to +20°C.

Upper Operating Limit (UOL): +110°C

Upper Destruct Limit (UDL): +>120°C

Table 10: Hot Step Stress Results

Chamber Set point (°C)	Pass/Fail	Comments
+20	Pass	Power Cycle – ABCD; DIO – ABCD; COM - ABCD; USB – ABCD Ethernet – ABCD; Flash - ABCD
+30	Pass	Power Cycle – ABCD; DIO – ABCD; COM - ABCD; USB – ABCD Ethernet – ABCD; Flash - ABCD
+40	Pass	Power Cycle – ABCD; DIO – ABCD; COM - ABCD; USB – ABCD Ethernet – ABCD; Flash - ABCD
+50	Pass	Power Cycle – ABCD; DIO – ABCD; COM - ABCD; USB – ABCD Ethernet – ABCD; Flash - ABCD
+60	Pass	Power Cycle – ABCD; DIO – ABCD; COM - ABCD; USB – ABCD Ethernet – ABCD; Flash - ABCD
+70	Pass	Power Cycle – ABCD; DIO – ABCD; COM - ABCD; USB – ABCD Ethernet – ABCD; Flash - ABCD
+80	Pass	Power Cycle – ABCD; DIO – ABCD; COM - ABCD; USB – ABCD Ethernet – ABCD; Flash - ABCD
+90	Pass	Power Cycle – ABCD; DIO – ABCD; COM - ABCD; USB – ABCD Ethernet – ABCD; Flash - ABCD
+100	Pass	Power Cycle – ABCD; DIO – ABCD; COM - ABCD; USB – ABCD Ethernet – ABCD; Flash - ABCD
+110	Pass	Power Cycle – ABCD; DIO – ABCD; COM - ABCD; USB – ABCD Ethernet – ABCD; Flash - ABCD
+120	Fail	Ethernet & Serial – All boards lost communications. Noticed that Board A rebooted itself. Others may have also. All LEDs lit, but Ethernet LED is blinking on UUTC & UUTD, but no packets are being sent.
+115	Fail	Receiving garbage data on COM port; rebooted All – Serial - Good (A); Ethernet – Good (A). BCD still no communication.
+110	Fail	Power Cycle – ACD good, B no communication, but 3.3 VDC good; DIO – ACD good, COM - ACD good; USB – ACD good, Ethernet – ACD good, B bad; Flash – ACD good,
+20	Pass	After rebooting, all UUTs appear normal.

Table 11: Temperatures Recorded During the Hot Temperature Step Stress (°C)

Set point (°C)	UUTA U8	UUTA U19	UUTB U8	UUTB U19	UUTC U8	UUTC U19	UUTD U8	UUTD U19	UUTA VDC12	UUTB VDC13
+20	22.2	21.5	21.4	20.1	22.0	22.8	24.9	23.4	3.300	3.318
+30	32.6	32.1	33.3	31.8	32.1	32.8	35.4	33.6	3.299	3.318
+40	42.4	41.9	43.5	42.0	42.0	42.7	44.1	42.8	3.298	3.317
+50	52.3	52.0	53.5	51.7	52.0	52.9	54.4	53.1	3.297	3.317
+60	62.1	61.9	63.1	61.6	61.9	62.7	64.5	63.1	3.296	3.317
+70	71.6	71.2	73.5	70.9	71.9	72.5	76.2	73.2	3.295	3.316
+80	81.1	80.9	82.1	80.4	81.5	82.4	84.3	82.8	3.294	3.316
+90	91.2	91.2	92.0	90.2	91.6	92.6	94.7	93.0	3.293	3.315
+100	100.8	100.8	101.5	99.6	101.6	102.7	104.8	103.1	3.291	3.315
+110	111.9	111.0	113.1	109.8	112.7	113.0	117.0	113.9	3.290	3.315
+120	118.5	118.5	117.4	115.3	120.5	120.7	125.0	122.2	3.290	3.315
+115	115.1	115.3	115.7	113.6	116.1	117.4	119.4	117.7	3.290	3.316
+110	110.7	110.8	112.1	110.3	111.6	113.0	114.6	113.1	3.291	3.315
+20	26.4	27.1	37.3	33.5	32.9	31.5	30.6	31.9	3.302	3.324

Note: Thermocouple Locations are documented in Table 6.

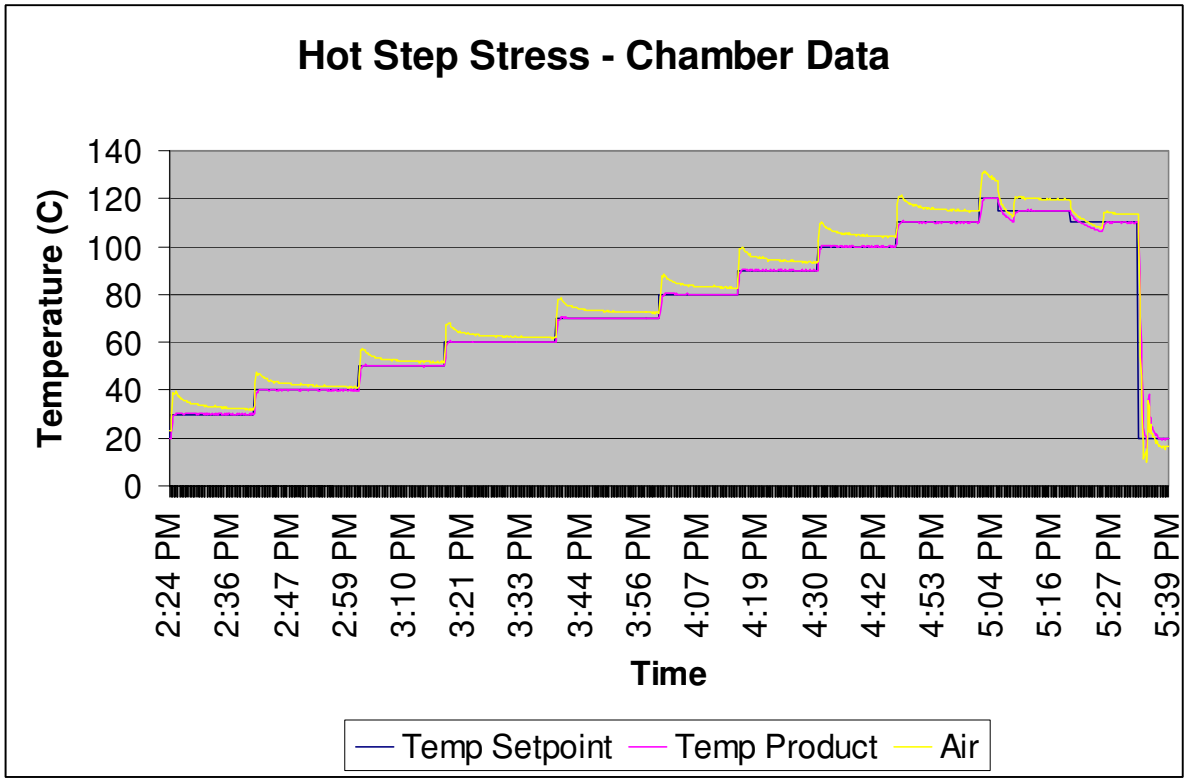


Figure 5: Hot Step Stress Test – Chamber Data

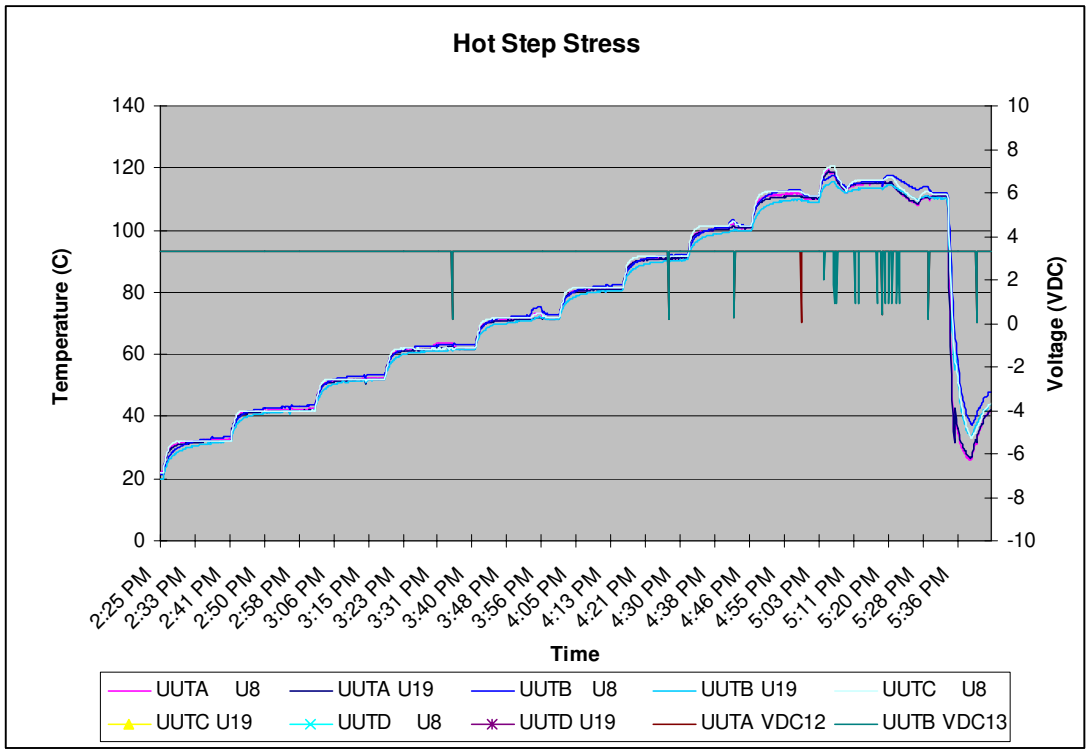


Figure 6: Hot Step Stress Test – Thermocouple and Voltage Readings

9.3 Rapid Thermal Transitions

The UUT was exposed to 5 rapid temperature cycles from –50°C to +110°C. The dwell time at each extreme was 5 minutes, and the thermal transition rate was set to the chamber maximum (> 60°C/min empty table). The actual maximum thermal transition rate on the product was 98.0°C in the cooling direction (65.5°C in the heating direction). This transition rate was calculated by averaging the thermal transition rate of each thermocouple measurement. The UUT was monitored for functionality throughout the rapid thermal transition process.

No problems were noted during this test.

Upper Set Point: +110°C

Lower Set Point: -50°C

Chamber Programmed Rate of Change: Not programmed;

Calculated Product Rate of Change: 98.0°C/min in the cooling direction.

Table 12: Rapid Thermal Cycle Results

Cycle	Chamber Set point (°C)	Pass/Fail	Comments
0	+20	Pass	Power Cycle – ABCD; DIO – ABCD; COM - ABCD; USB – ABCD Ethernet – ABCD; Flash - ABCD
1	Transition		
1	-50	Pass	Power Cycle – ABCD; DIO – ABCD; COM - ABCD; USB – ABCD Ethernet – ABCD; Flash - ABCD
1	Transition		
1	+110	Pass	Power Cycle – ABCD; DIO – ABCD; COM - ABCD; USB – ABCD Ethernet – ABCD; Flash - ABCD
1/2	Transition		
2	LOL	Pass	Power Cycle – ABCD; DIO – ABCD; COM - ABCD; USB – ABCD Ethernet – ABCD; Flash - ABCD
2	Transition		
2	UOL	Pass	Power Cycle – ABCD; DIO – ABCD; COM - ABCD; USB – ABCD Ethernet – ABCD; Flash - ABCD
2/3	Transition		
3	LOL	Pass	Power Cycle – ABCD; DIO – ABCD; COM - ABCD; USB – ABCD Ethernet – ABCD; Flash - ABCD
3	Transition		
3	UOL	Pass	Power Cycle – ABCD; DIO – ABCD; COM - ABCD; USB – ABCD Ethernet – ABCD; Flash - ABCD
3/4	Transition		
4	LOL	Pass	Power Cycle – ABCD; DIO – ABCD; COM - ABCD; USB – ABCD Ethernet – ABCD; Flash - ABCD
4	Transition		
4	UOL	Pass	Power Cycle – ABCD; DIO – ABCD; COM - ABCD; USB – ABCD Ethernet – ABCD; Flash - ABCD
4/5	Transition		
5	LOL	Pass	Power Cycle – ABCD; DIO – ABCD; COM - ABCD; USB – ABCD Ethernet – ABCD; Flash - ABCD
5	Transition		
5	UOL	Pass	Power Cycle – ABCD; DIO – ABCD; COM - ABCD; USB – ABCD Ethernet – ABCD; Flash - ABCD
	+20	Pass	

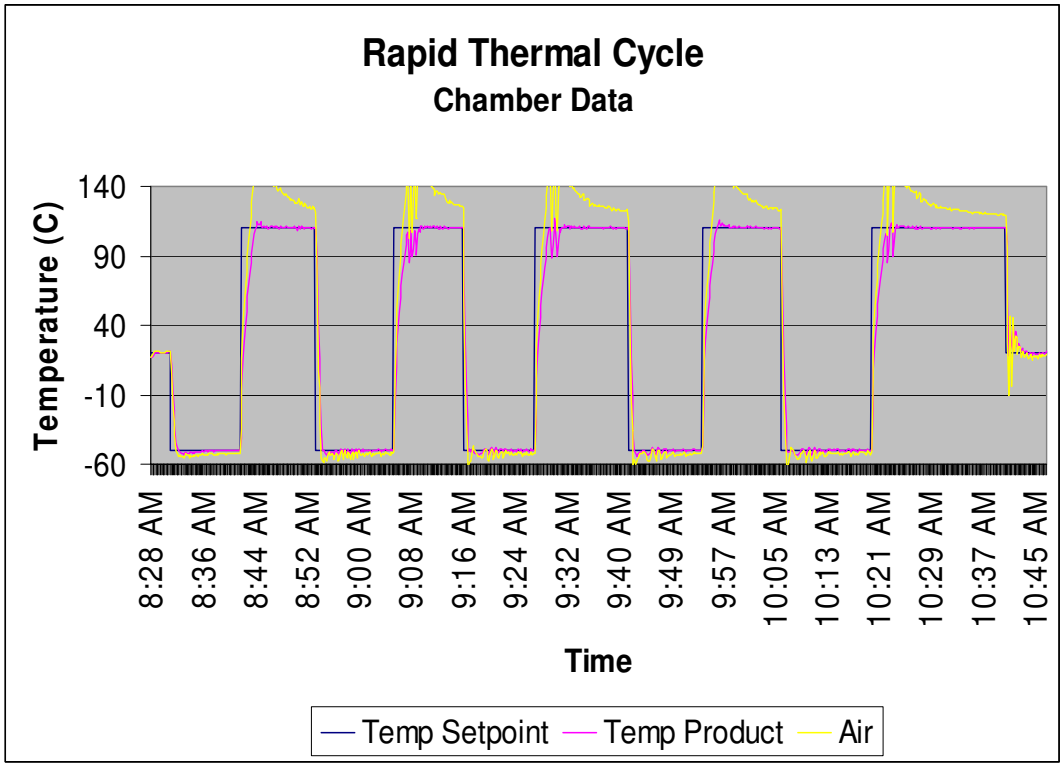


Figure 7: Rapid Thermal Cycle Test – Chamber Data

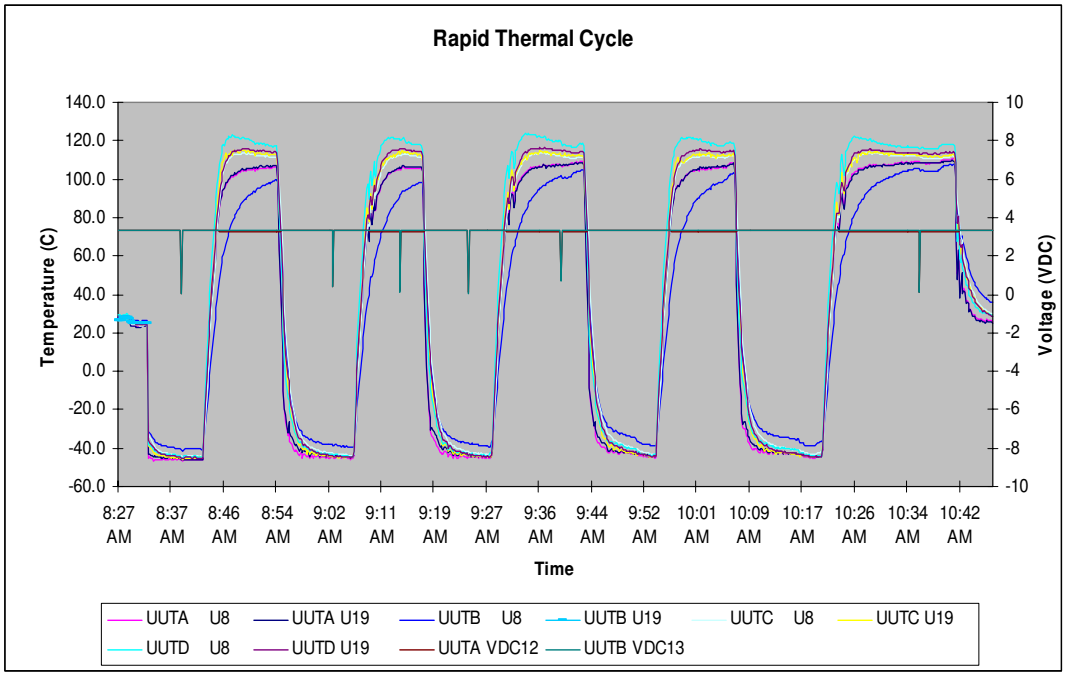


Figure 8: Rapid Thermal Cycle Test – Thermocouple and Voltage Readings

9.4 Vibration Step Stress

The vibration step stress began at a set point of 5 Grms and was increased in 5 Grms increments. The dwell time at each set point was 10 minutes. After the 30 Grms level, the vibration was decreased to 5 Grms to determine if a failure occurred that was not detected at the higher vibration level. If a failure was not detected during this "tickle vibration", the vibration was increased to the next level. The temperature was set to 25°C. The UUT was monitored for functionality throughout the test.

The following abnormalities were noted during the test –

1. At 10 Grms and 20 Grms, there were some cases in which the UUTs would reboot by themselves. This may have been due to the vibration affecting the power supply connector at the PCB. (Combined Environment Testing on Day 3 used a soldered power connection to the UUT in lieu of the power connector. See results in paragraph 9.6.)
2. At 30 Grms and higher, failures were seen related to USB communication.
3. At 40 Grms and higher, UUTs started rebooting by themselves. Also saw one instance of the Ethernet test failing.

Vibration Operating Limit (VOL): 25 Grms
Vibration Destruct Limit (VDL): >55 Grms

Table 13: Vibration Step Stress Results

Chamber Set point (Grms)	Pass/Fail	Comments
5	Pass	Power Cycle – ABCD; DIO – ABCD; COM - ABCD; USB – ABCD Ethernet – ABCD; Flash - ABCD
10	Pass	UUTB & UUTC rebooted during vibration. Power Cycle – ABCD; DIO – ABCD; COM - ABCD; USB – ABCD Ethernet – ABCD; Flash - ABCD
15	Pass	Stopped test in middle of dwell to adjust airflow ducting. Power Cycle – ABCD; DIO – ABCD; COM - ABCD; USB – ABCD Ethernet – ABCD; Flash - ABCD
20	Pass	Lost communication with UUTD. Rebooted with no vibration, UUTD recovered. Power Cycle – ABCD; DIO – ABCD; COM - ABCD; USB – ABCD Ethernet – ABCD; Flash - ABCD
25	Pass	Power Cycle – ABCD; DIO – ABCD; COM - ABCD; USB – ABCD Ethernet – ABCD; Flash - ABCD
30	Fail	Power Cycle – ABCD; DIO – ABCD; COM - ABCD USB – A B C-failed, D-failed; Stopped vib, C still failing, D passing. Stopped test – checked connections – C still failing. Verified USB cable and flash devices are okay. Will continue in test. Ethernet – ABCD; Flash - ABCD
35	Fail	Power Cycle – ABCD; DIO – ABCD; COM - ABCD USB – A & B okay, C & D – Failed. Stopped vib – both still failing. Ethernet – ABCD; Flash - ABCD
5	Fail	Except for C & D USB comm..
40	Fail	Power Cycle – ABC; D hung while powering up; rebooted itself and came up. DIO – ABCD; COM - ABCD USB – A&B okay; C&D-failed. Ethernet – A passed, B failed; CD passed; Flash - ABCD
5	Fail	USB – C passes and D fails.; Ethernet - B passes;
45	Fail	Power Cycle – A & C are continually rebooting; B – no response; D - okay DIO – D – passed; COM - D – passed; USB – D – failed; Ethernet – D - passed; Flash – D – passed;
0	Fail	Power Cycle – A - pass, B is continually rebooting – possibly intermittent power connection – reconnected – now okay – replaced power supply/cable; C & D – pass DIO – A, C,D; B now passing; COM - A, C,D; B now passing USB – A, C & D – Fail. Power cycled D – now passes. C is still failing. Ethernet – A,C, D; B now passing; Flash – A,C,D; B now passing
50	Fail	Power Cycle – A & B – continually rebooting; D not responding; C okay. DIO – C; COM - C; USB – C fails; Ethernet – C; Flash - C
0	Pass	Power Cycle – ABCD DIO – ABCD; (A failed initially, but found connector had lifted – reseated) COM - ABCD; USB – ABCD; Ethernet – ABCD; Flash - ABCD
55	Fail	A,B, C are continually rebooting; D is not responding.
0	Fail	Power Cycle – B is rebooting, but after a few minutes, stopped rebooting – working fine now, ACD pass. DIO – ACD; COM - ACD; USB – A – fails. CD pass. Ethernet – ACD; Flash –ACD
0	Pass	Moved TC12 from UUTA 3.3VDC to UUTB 5.0 VDC. (402pm); All UUTs – now passing.
55	Fail	Power Cycle – C not responding; ABD DIO – A failed; (found loose 14 pin ribbon cable connector); BD COM - ABD; USB – ABD – failed; Ethernet – ABD; Flash – ABD
0	Pass	C is continually rebooting – stopped after reseating the power connector;

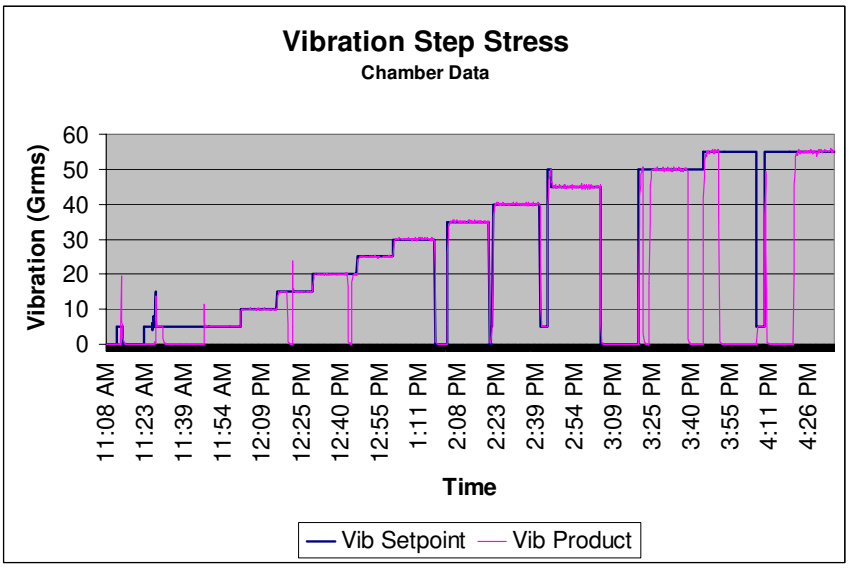


Figure 9: Vibration Step Stress Test – Chamber Values

9.5 Vibration Measurements

Vibration levels were measured at three product locations during the vibration step stress. The vibration measurements on the product were taken using a QualMark spectrum analyzer. The bandwidths used to calculate the Grms levels on the product were 2Hz to5,000 Hz using a digital filter at 5,000 Hz. During each vibration step, a power spectral density plot was taken showing the calculated Grms level on the product and the distribution of energy over the desired frequency bands 2 Hz to 5,000 Hz. The Grms levels measured on the UUTs are shown in the table below and the spectral density plots are located in Appendix B (See Table 7 for accelerometer locations).

Table 14: Vibration Levels Measured During Vibration Step Stress (Grms)

Chamber Set point	Channel 2 UUTB 2 Hz-5k Hz	Channel 3 UUTD 2 Hz-5k Hz	Channel 4 Table 2 Hz-5k Hz	Channel 5 UUTA 2 Hz-5k Hz
5	5.62	2.89	6.58	4.71
10	9.91	6.85	13.58	7.71
15	13.76	9.41	19.69	11.58
20	18.53	13.53	26.16	15.28
25	23.36	15.97	30.26	19.61
30	26.83	19.86	38.12	22.88
35	30.54	22.13	45.15	26.16
40	34.14	24.89	52.05	30.71
45	38.18	29.49	57.53	34.67
50	44.11	32.01	64.72	40.32
55	57.32	36.92	71.43	30.41

Table 15: Transmissibility Ratio (Energy at Product (response) vs. Input Energy)

Transmissibility of Energy from Vibration Table to Product			
Chamber Setpoint	Channel 2 UUTB Z axis Response	Channel 3 UUTD Z axis Response	Channel 5 UUT A Z axis Response
5	1.193	0.614	1.397
25	1.191	0.814	1.543
55	1.885	1.214	2.349

Note: Calculation made using the 2Hz – 5kHz frequency band.

9.6 Combined Environment

The UUT was exposed to 10 1/2 rapid temperature cycles starting at -50°C to +110°C and ending at -85°C and +120°C. The vibration level was set to 5 Grms for the first temperature cycle and then increased in 5 Grms increments before each additional cycle through cycle 5. For cycles 6 through 11, vibration levels started at 25 Grms and ended at 65 Grms. The dwell time at each temperature extreme was 10 minutes and the thermal transition rate was set to the chamber maximum (> 60°C/min. empty table). The actual thermal transition rate on the product was 98°C in the cooling direction (This transition rate was calculated during the rapid thermal transition process). The UUT was monitored for functionality throughout the combined environment process.

The following abnormalities were noted during the test –

1. Initially, at low vibration levels the UUTs kept rebooting. The problem was due to the intermittent power connections at the PCB/PS connector interface. The connectors were removed and the PS wires were soldered directly to the PCB pins. This resolved that problem.
2. During the first two cycles, the upper temperature limit was +110°C - but at that level there were numerous problems attempting to communicate with the UUTs. When the temperature was dropped back to +100°C, communication was reestablished. Root cause of this problem needs to be investigated.
3. At the cold portion of the temperature cycle with vibration, problems with the USB Test were seen. In one case the problem cleared when the USB cables were reseated in the PCB connector. In all cases, the problems cleared when the vibration was turned off and the temperatures returned to ambient. The USB connector cannot handle vibration – this is an industry known problem. This problem was initially seen in the vibration test at 30 Grms.
4. On the 11th cycle at -85°C and 65 Grms (very extreme levels), UUTs A, B, & D passed all tests, but the test diagnostics could not communicate with UUTC. Upon return to ambient, UUTC began to work, but the Green LED on the PCB was very weak. As the PCB warmed up the LED returned to normal. UUTC then passed all tests. This needs further investigation.

Table 16: Combined Environment Results (Cycles 1 through 5)

Cycle	Chamber Set point (°C)	Chamber Set point (Grms)	Pass/Fail	Comments
0	+20	0	Pass	Power Cycle – ABCD; DIO – ABCD; COM - ABCD; USB – ABCD Ethernet – ABCD; Flash - ABCD
1	Transition	5	Fail	C is periodically rebooting – power connector issue.
1	-50	5	Fail	Power Cycle – ABD; C is periodically rebooting – power connector issue. DIO – ABD; COM - ABD; USB – ABD Ethernet – ABD; Flash - ABD
1	Transition	5	Fail	A is periodically rebooting – power connector issue.
1	+110	5	Fail	No communication with any UUT. Turned off vib. Power cycled again; A Passed all tests, but cannot talk to BCD. A then rebooted gain.
	20	0	Pass	A – as temp drops UUT stops rebooting; Power Cycled – all UUTs passed.
				THU, 2/23 – soldered p/s connections to PCB pins.
1/2	Transition	10	Pass	
2	-50	10	Pass	Power Cycle – ABCD; DIO – ABCD; COM - ABCD; USB – ABCD Ethernet – ABCD; Flash - ABCD
2	+110	10	Fail	A passes all tests, but BCD are not responding.
	+110	0	Fail	Rebooted; Still BCD are not responding. Next cycle, will only go to +100 C.
3	-50	15	Pass	Power Cycle – ABCD; DIO – ABCD; COM - ABCD; USB – ABCD Ethernet – ABCD; Flash - ABCD
3	+100	15	Pass	Power Cycle – ABCD; DIO – ABCD; COM - ABCD; USB – ABCD Ethernet – ABCD; Flash - ABCD
4	-50	20	Fail	Power Cycle – ABCD; DIO – ABCD; COM - ABCD USB – A & D passed; B&C –Failed; Ethernet – ABCD; Flash - ABCD
	-50	0	Fail	USB – B&C still fail.
4	+100	20	Pass	Power Cycle – ABCD; DIO – ABCD; COM - ABCD; USB – ABCD Ethernet – ABCD; Flash - ABCD
5	-45	20	Fail	USB – B&C still fail.
	-50	25	Fail	Power Cycle – ABCD; DIO – ABCD; COM - ABCD USB – A passed; BC&D –Failed; Ethernet – ABCD; Flash - ABCD
5	+100	25	Fail	Power Cycle – ABCD; DIO – ABCD; COM - ABCD USB – ACD passed; B–Failed; Ethernet – ABCD; Flash - ABCD
	+20	0	Fail	USB – B still failing. Reseated USB connectors, now passing.

Table 17: Combined Environment Results (Cycles 6 through 10)

Cycle	Chamber Set point (°C)	Chamber Set point (Grms)	Pass/Fail	Comments
6	Transition	25		
6	-55	25	Fail	Power Cycle – ABCD; DIO – ABCD; COM - ABCD USB – A&B passed; C&D failed; Ethernet – ABCD; Flash - ABCD
6	+100	25	Fail	Power Cycle – ABCD; DIO – ABCD; COM - ABCD USB – A&C passed; B&D failed Ethernet – ABCD; Flash - ABCD
7	-60	25	Fail	Power Cycle – ABCD; DIO – ABCD; COM - ABCD USB – A – passed; BCD – failed Ethernet – ABCD; Flash - ABCD
7	+100	25	Fail	Power Cycle – ABCD; DIO – ABCD; COM - ABCD USB – ABC-passed; D failed Ethernet – ABCD; Flash - ABCD
8	-65	25	Failed	Power Cycle – ABCD; DIO – ABCD COM - ABD – passed; C – failed. USB – A&B – passed; C&D - failed Ethernet – ABCD; Flash - ABCD
8	+100	25	Pass	Power Cycle – ABCD; DIO – ABCD; COM - ABCD; USB – ABCD Ethernet – ABCD; Flash - ABCD
9	-70	25	Fail	Power Cycle – ABCD; DIO – ABCD; COM - ABCD USB – A – passed; BCD – failed; Ethernet – ABCD; Flash - ABCD
9	+100	25	Pass	Power Cycle – ABCD; DIO – ABCD; COM - ABCD; USB – ABCD Ethernet – ABCD; Flash - ABCD
10	-80	55	Fail	Power Cycle – ABCD; DIO – ABCD; COM - ABCD USB – A – passed; BCD – failed; Ethernet – ABCD; Flash - ABCD
10	+120	55	Fail	A passed all tests; BC&D – cannot communicate with.
11	-85	65	Fail	AB&D- passed all tests; C – cannot communicate with.
	+20	0	Pass	C – Green LED is much dimmer than Green LED on other UUTs, but it returned to normal during the post test inspection – warmed up? Several of the serial connectors had their locking screws back out, but connector remains connected. Power Cycle – ABCD; DIO – ABCD; COM - ABCD; USB – ABCD Ethernet – ABCD; Flash - ABCD

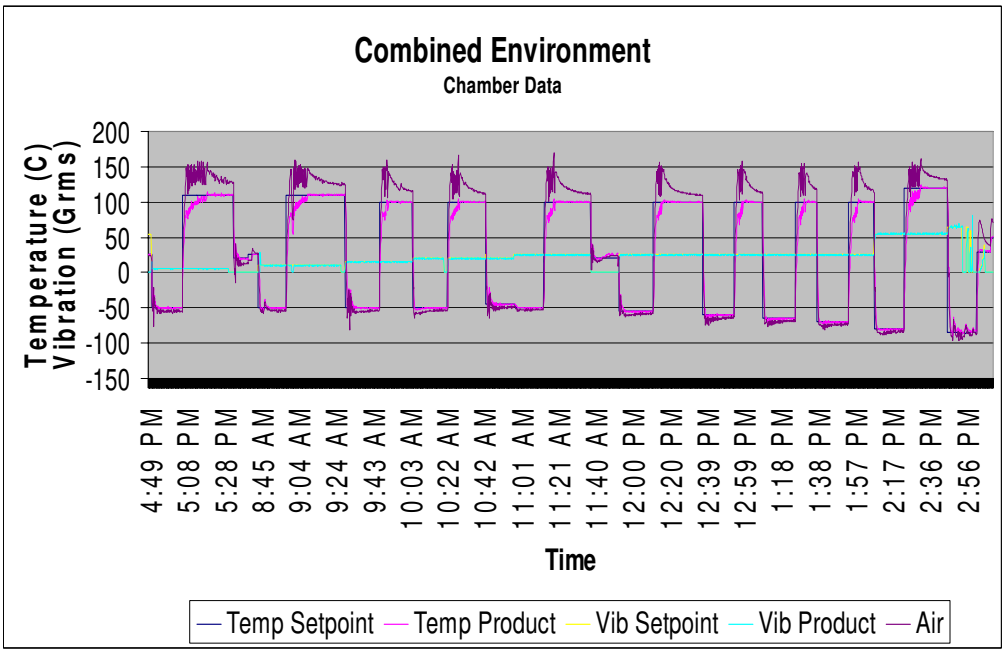


Figure 10: Combined Environment Test – Chamber Data

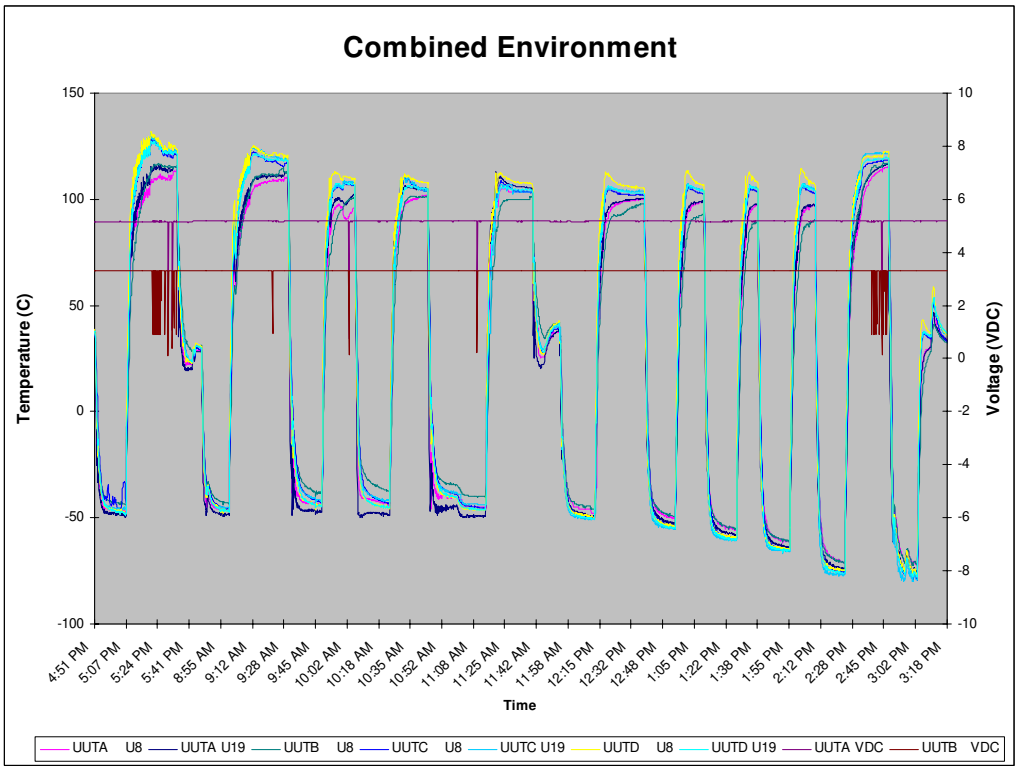


Figure 11: Combined Environment Test – Temperature and Voltage Data

10. Synopsis/Recommendations

The UUTs were subjected to thermal and vibration stresses to determine the product's operating and destruct limits, as well as, to expose potential design and manufacturing related weaknesses. During testing it was determined that potential weaknesses and failure modes were exposed due to product design and/or manufacturing. It is recommended that these weaknesses be examined for root cause, corrected, and then re-tested to confirm that the corrective action improved product robustness.

Based on the results of the test, we recommend that you -

a) Cold Step Stress Test - Conduct some cold temperature tests to see if the corrupted data in the flash memory can be recreated. When even colder temperatures were seen in the Combined Environment Test, no problems were seen.

b) Hot Step Stress Test – Investigate to determine the cause of the failure to communicate with the UUTs at 120°C. A similar problem was seen during the Combined Environment Test at 110°C.

c) Vibration Step Stress Test – Evaluate how power will be applied to this single board computer in the LGC Wireless application. There obviously was a problem using the Technologic Systems power connector in a vibration environment.

d) Vibration Step Stress Test – Investigate the USB connection/interface to confirm the assumption that the USB test failures were due to that interface.

e) Combined Environment Test – Investigate the cause of the dim Green LED during the testing at -85°C and 65 Grms (very extreme levels).

Appendix A - Photographs

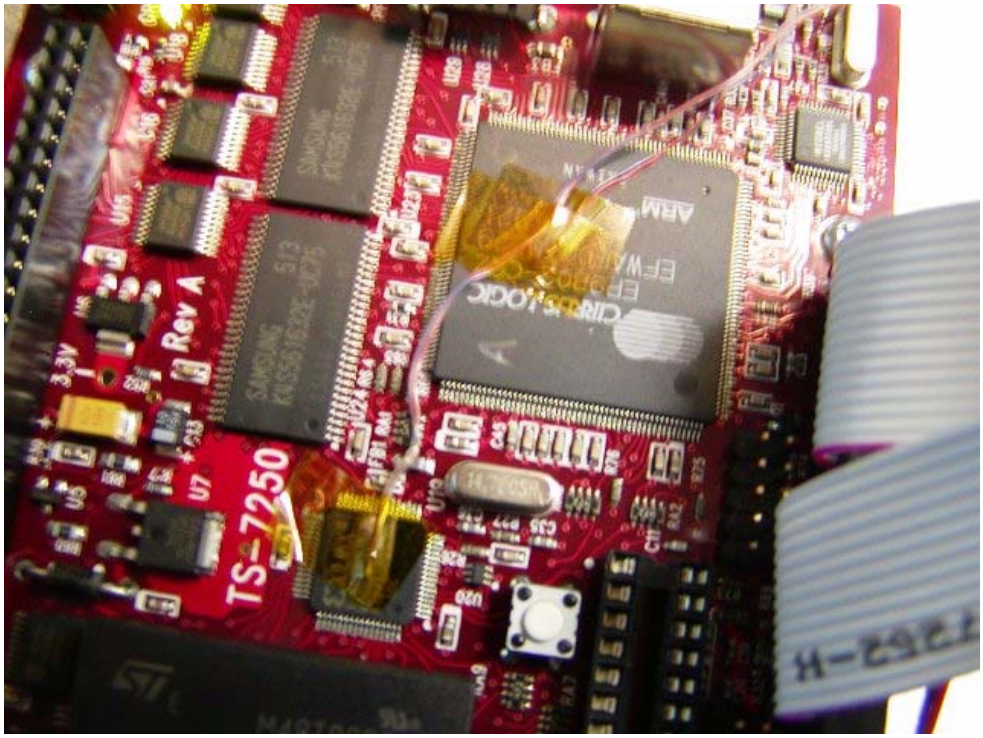


Figure A.1: Thermocouple Locations

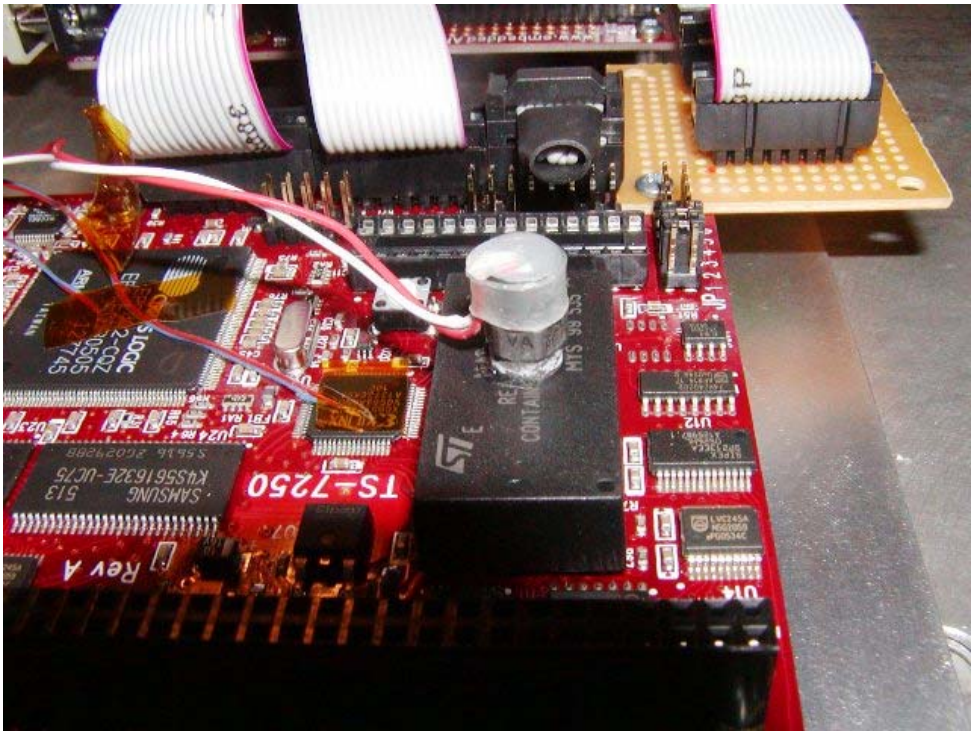


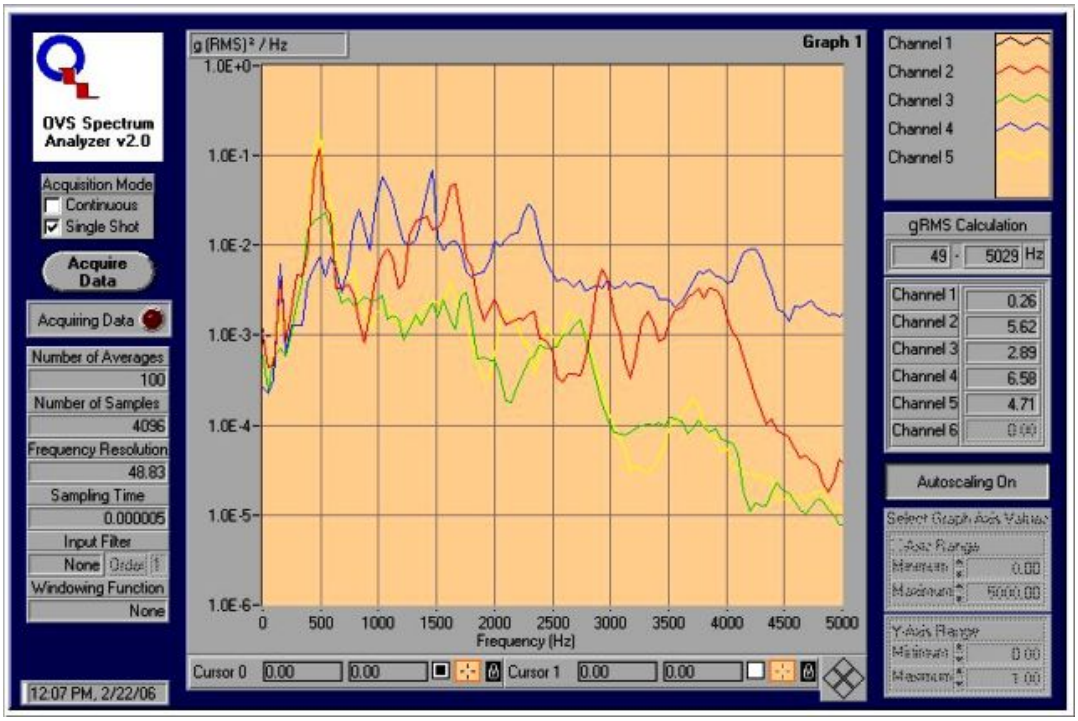
Figure A.2: Typical Accelerometer Placement

Appendix B - Vibration Plots

Spectrum Analyzer Channel Assignment		
Channel	**Axis**	**Location or Description**
5	Z	Mounted on UUT#A
2	Z	Mounted on UUT#B
3	Z	Mounted on UUT#D
4	Z	Mounted underneath the vibration table at center.

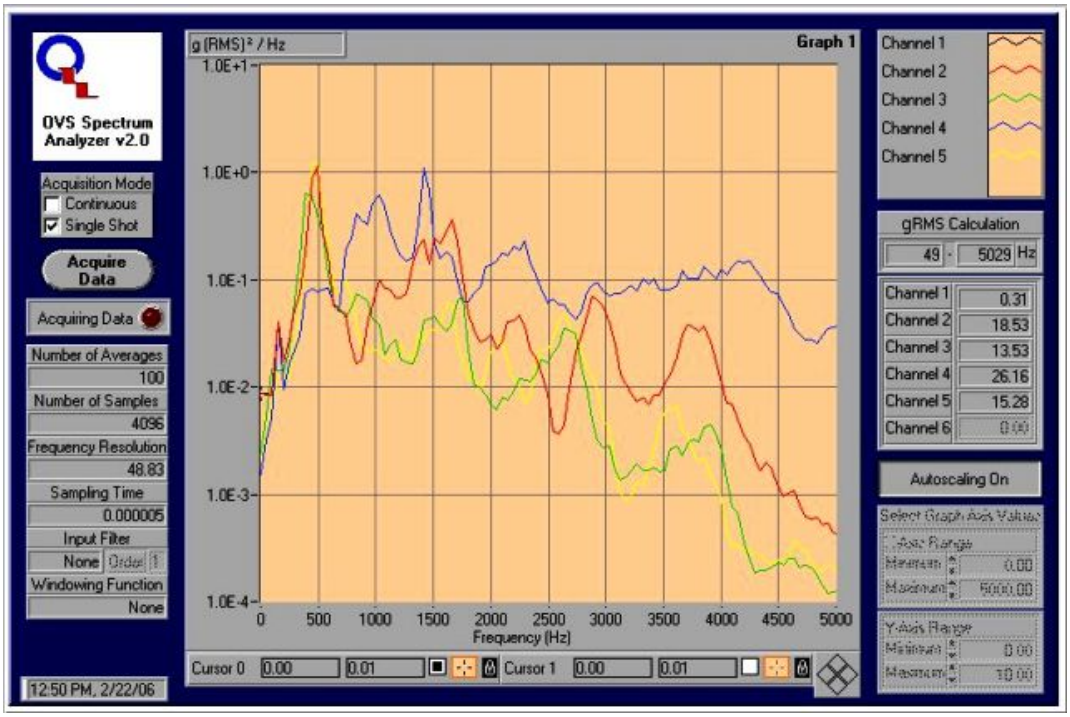
Note: The X-axis runs through the chamber doors, the Y-axis runs from the access portal to air plenum, and the Z-axis is vertical to the vibration table.

Vibration Plot - 5 Grms

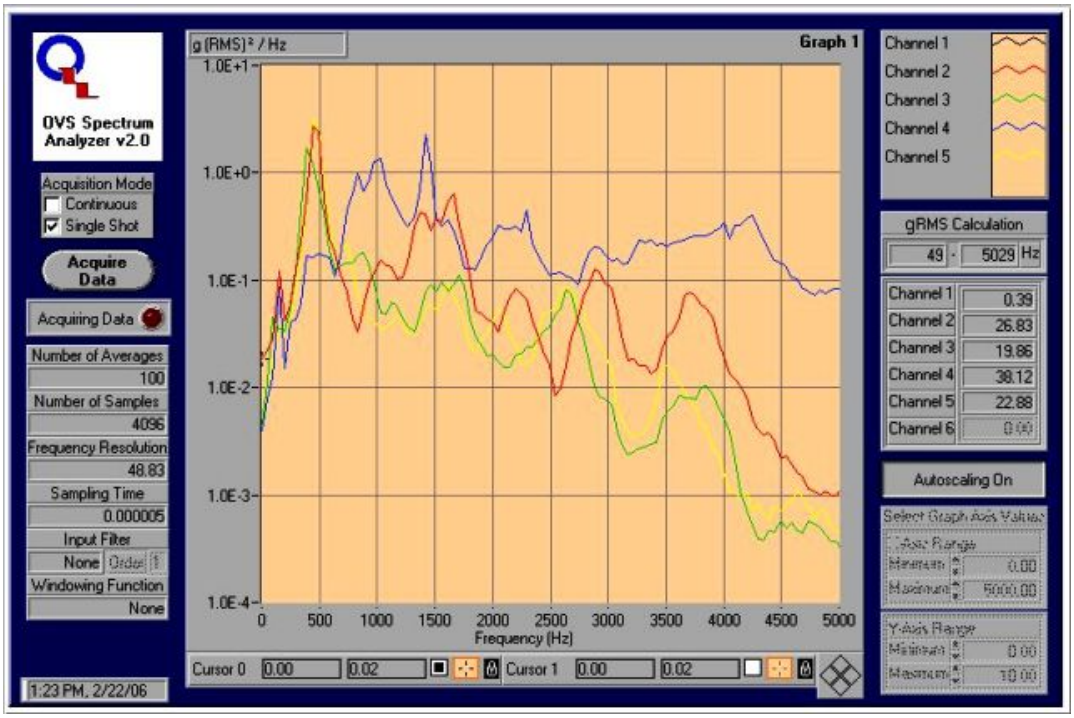


Appendix B - Vibration Plots

Vibration Plot - 20 Grms

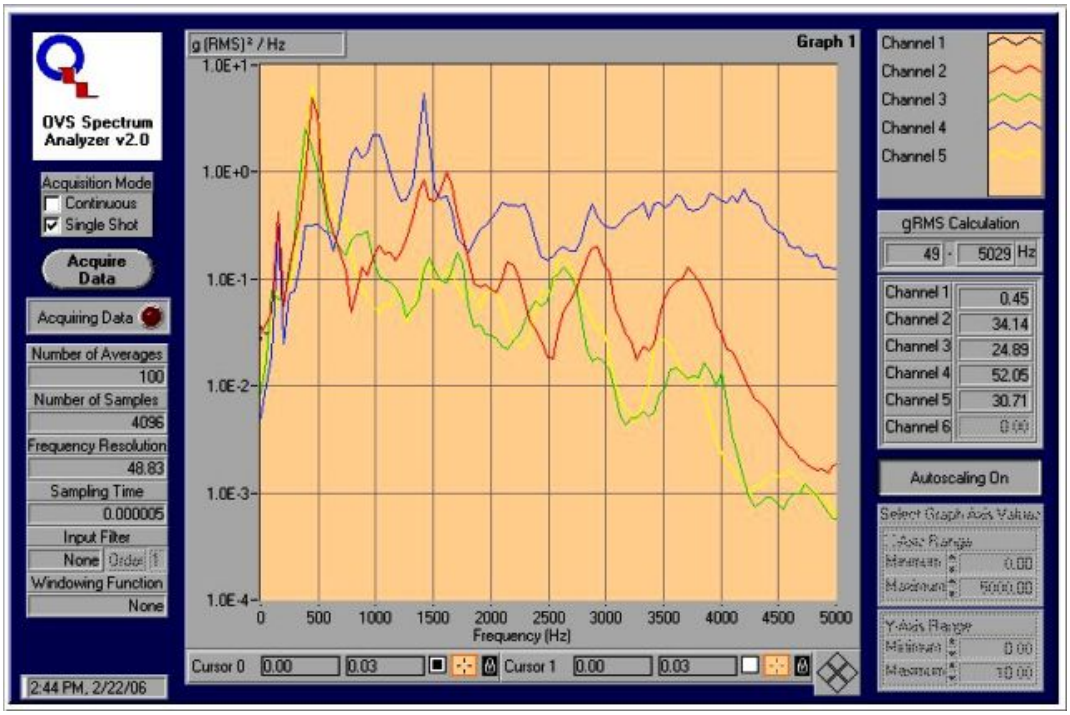


Vibration Plot - 30 Grms



Appendix B - Vibration Plots

Vibration Plot - 40 Grms



Vibration Plot - 55 Grms